384-element detector is an energy spectrum detector only; and cannot meet the needs of coherent scattering application which acquires the timing spectrum. Obtaining the timing spectrum for momentum energy detection requires a large area image detector which has a large number of pixels and the proper control of charge transfer. Photon correlation processing in real time mode is also needed. Research activities on the coherent scattering detector design will be discussed in Chapter 4.

3.3 Maia 96-Element Detector Design

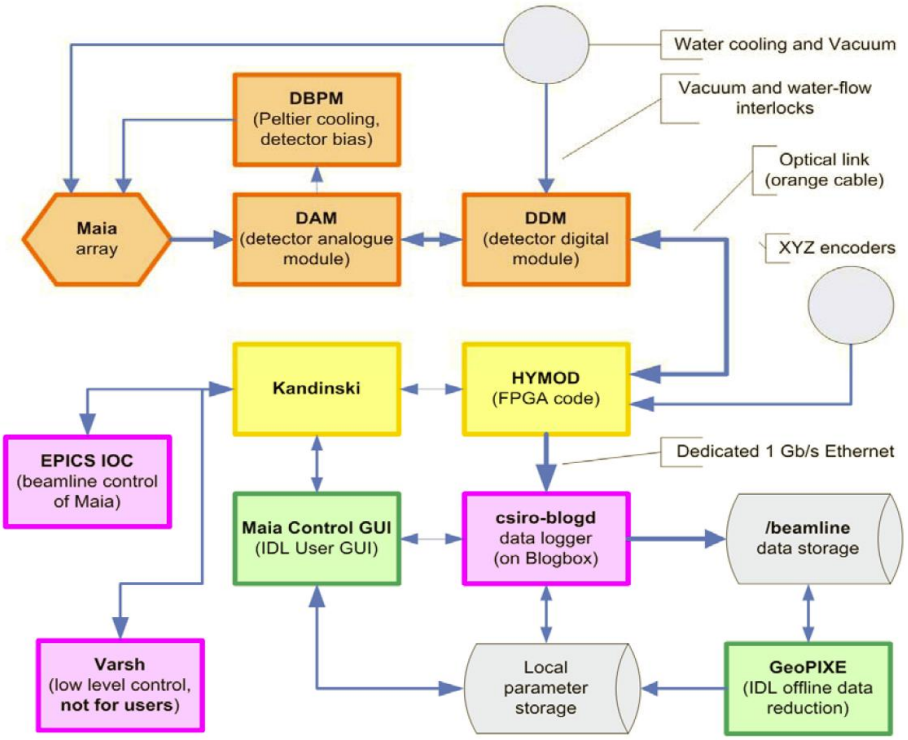
3.3.1 Introduction

Prior to this work, motivated by providing the MCA function for each element of photodiode, the Maia 384-element detector system was developed as a collaboration between BNL and CSIRO [26] but the detector analog board suffered from several serious problems such as high noise, high minimum detectable energy limit, spectrum peak drifting at different counting rates, etc. In this project, the 96-element detector board (DAM in Maia system) was re-designed from scratch to get better detector parameters.

The Maia system architecture and hardware layout are displayed in Figure 3.20. The signal acquisition of Maia system starts with DAM (Detector Analog Module) board, in which the photodiode array collects the X-ray photon and converts it to charge signal, which is converted to Gaussian pulse with defined shaping time by the HERMES chip in the next step. Finally the pre-shaped pulse is processed in SCEPTERs and the E/T (Event/Time) and address (position of pixels) information is extracted from each channel and sent to the DDM (Detector Digital Module) board. In DDM board, E/T signal is converted to digital signal by high speed ADC circuit. All these digital data such as

energy, timing, pixel address are either real-time data processed in DDM or transferred to HYbrid MODular processor（HYMOD) [26] module via optical ribbon cables. The HYMOD module collects the data of sample scanning position in X-Y space and combines it with the data from DDM to form the “BLOG” data. The “BLOG” data finally is passed to disk and stored (used to produce the full energy spectra vs. x-y or energy for example). The data readout rate between DAM and system is expected to handle a maximum of 30M counts/second (based on the maximum read request clock rate). The Maia system diagram, displayed in Figure 3.20, contains Detector Analog Module (DAM), which has the multi-pixels sensor and related pulse processing circuit. The Detector Digital Module (DDM) collects the timing, energy, counts, location of pixels data from DAM board. It connects with HYMOD with a 1Gbits Ethernet fiber. The HYMOD serves the interface between the computer which has huge storage capacities and the detector board. The system also has the control interface of EPICS IOC to beamline for energy scan, motor control etc. purpose. Maia control GUI can collect data in real time (during measurements) both from the detector system and the beamline EPICS system.

(a)



(b)

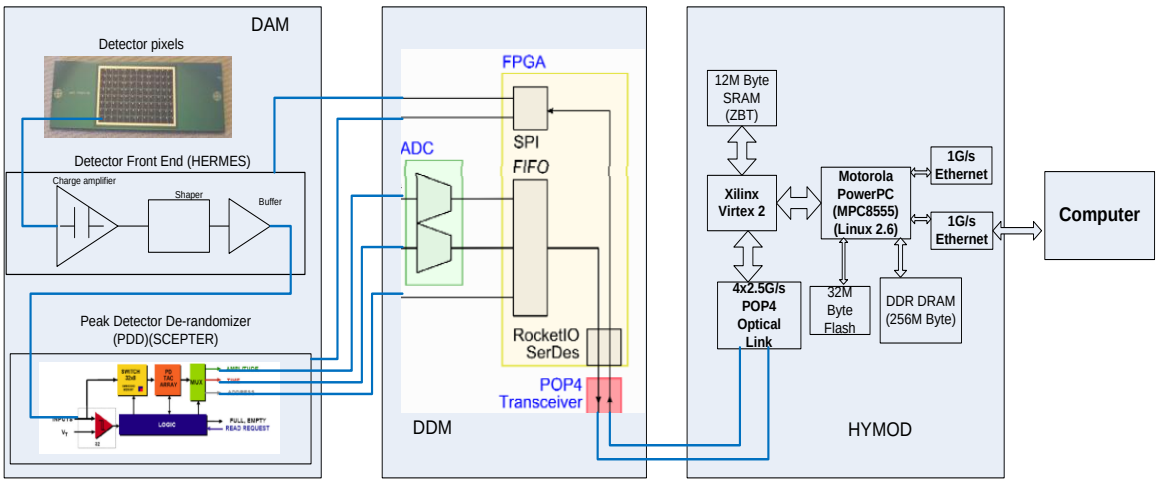
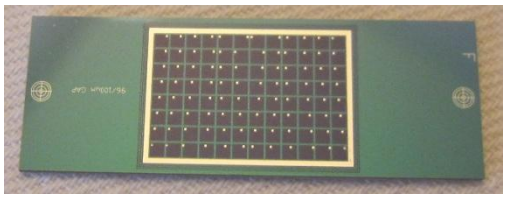


Figure 3.20 (a) Maia system architecture. (b) Maia system hardware layout.

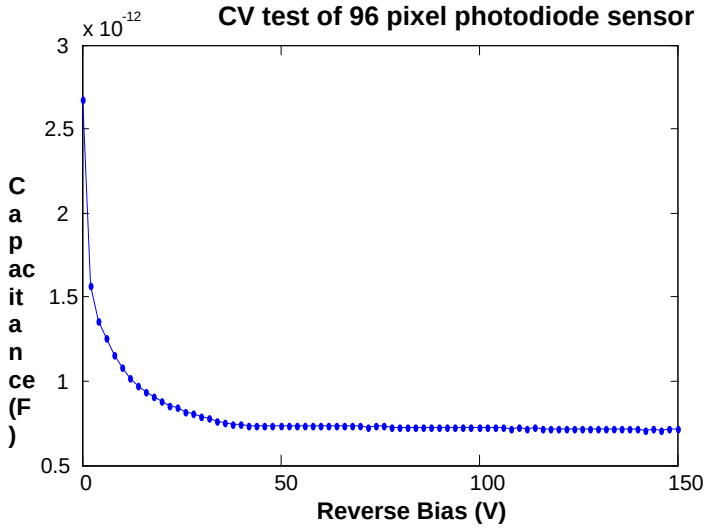
The DAM has the X-ray sensor, pre-amplifier (HERMES chips), peak/timing detector along with address output (SCEPTER chips), ADC for temperature reading and baseline reading, DAC for sensor bias control, power on/off control etc. It is the critical part for the whole detector system. The noise level of the board decides if the high energy resolution and a low minimum detectable energy can be achieved.

As displayed in Figure 3.21(a), the X-ray sensor array used in this detector is a photodiode array which has 96 elements. The size of pixel is 1 mm x 1 mm; the elements are arranged in 8 * 12 matrix structure surrounded by a guard ring. Displayed in Figure 3.21(b), the CV characteristics of the sensor measured at room temperature before mounted on the board indicates that the photodiode becomes fully depleted at a reverse bias of 43 volts. Figure 3.21(c) shows that the IV test data measured at room temperature before mounting on the board indicating that the reverse leakage current saturates at ~1 nA limiting the effectiveness of the sensor. It is, obviously, necessary to reduce the leakage current.

(a)



(b)



(c)

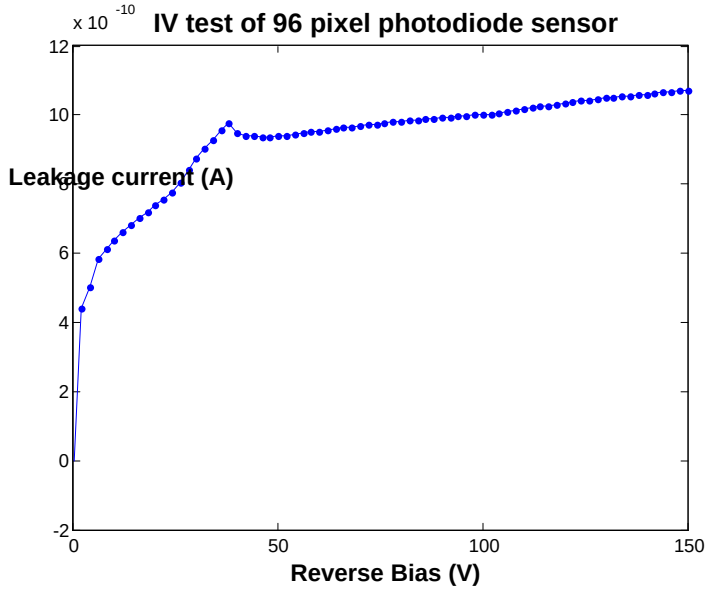


Figure 2.21 (a) 96 pixels photodiode sensor. (b) Bottom left corner pixel C-V curve. (c) Bottom left corner pixel I-V curve.

The Scepter ASIC [21], displayed in Figure 3.22, is designed to process pulses from 32 inputs. It has 5 modules, where the 32-channel comparator counts the photons if it is above the V_t threshold, the trigger to other modules and data valid signal to outside will be generated in logic part after; logic part controls all the registers for each modules and provides the communication links with outside circuit; the Switch selects a maximum of 8 channels out of 32 for the 8 peak detector (PD) and time amplitude convertor (TAC) array; the pulse amplitude and shaping time information from PD and TAC and the address will be passed to multiplexer (MUX) module to be sequentially readout. The ASIC provides 2 analog signals which are peak and time of pulse per event to the fast external ADC. The 8 peak detectors act as derandomizing analog memory, which could record 8 channels at the same time and to be read out with the readout clock in serials.

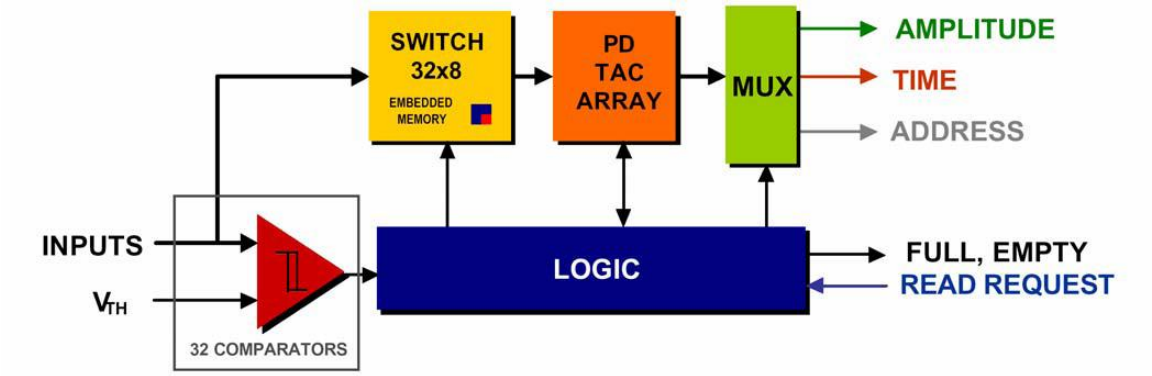


Figure 3.22 SCEPTER ASIC architecture [21]

3.3.2 Design

In order to achieve low noise, the following design approaches are used. First, the sensor is bonded with HERMES chips with 96 bonding wires (25 micron diameter) which are

thermally conductive. The heat of the board can be transferred to sensors though these wires. Hence, circuit architecture is simplified to reduce the number of devices populated on the board to reduce the heat from the total power consumption. The previous version of 384-element detector use the star network for the token pass of serial peripheral interface bus where a complex programmable logic device (CPLD) provides the token pass for each devices. In this development, a daisy chain is used and the token pass is passed from one device to another, the CPLD is consequently eliminated.

Secondly, the peak detector (PD) and timing detector (TD) of SCEPTER drives the differential driver directly in the previous version, where the differential driver (EL5371) only has 300 kΩ. It was suspected that the SCEPTER may not be able to drive the load. A fast FET operational amplifier (AD8066) was added between SCEPTER and differential driver and tested. It was found the output amplitude of SCEPTER increased significantly in the new circuit. Furthermore, the buffer improved the timing characteristic because of the input capacitance of buffer. It was concluded that a buffer is needed.

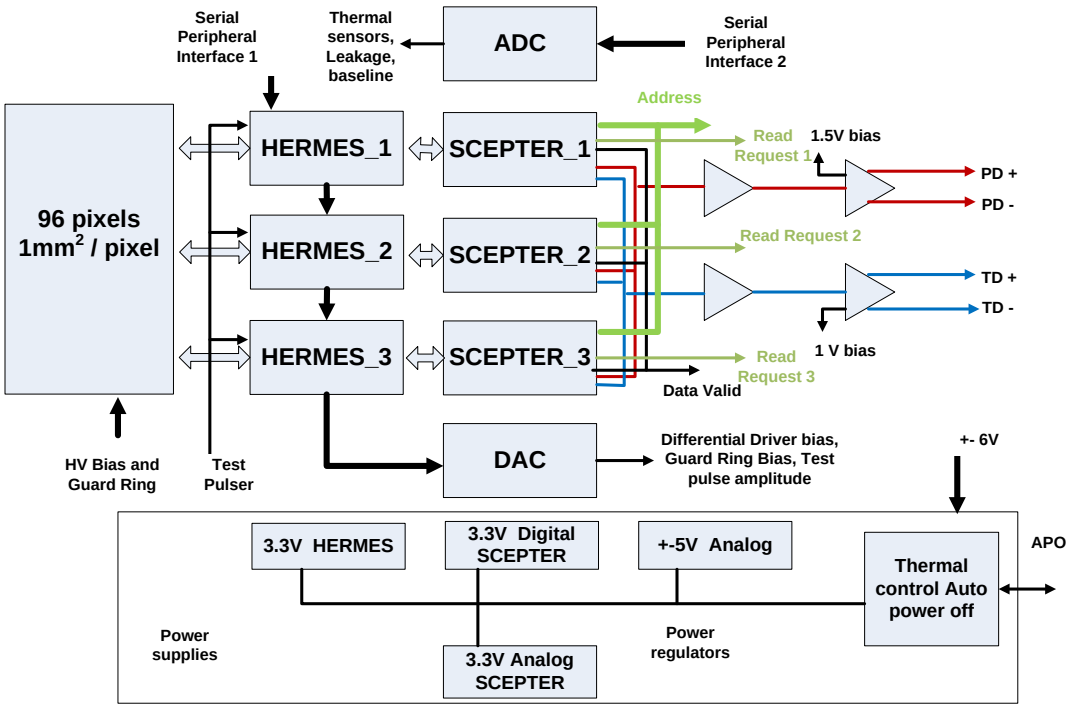
Thirdly, Maia system can provide a 10 MHz readout clock, which means the PD and TD signal delay between SCEPTER and high speed ADC needs to be < 100/3 ns. This revealed the bottle neck of total counting rate later. Consequently the differential driver was replaced with a high speed version of EL5374 which has bandwidth twice as big as the one of EL5371.

Fourthly, an auto power off circuit was added in the circuit where the LM56 thermostat is selected to monitor the temperature of the PWB. When the PWB temperature is above the threshold in case that the cooling system breaks down, the

thermostat will turn off all the power circuit of the board. This will prevent the sensor and detector from overheating. The latest version of SCEPTER (Version 7) was used in this design which has higher power consumption (110mW) because more features are added; this makes the thermal control more important. Also, straight forward bonding pads are used on the die; the corresponding footprint needs to be redesigned.

The finalized schematic design is displayed in Figure 3.23 (a). In the layout design, which is a critical process to eliminate the noise problem, high speed low noise layout design rules are followed. Twelve layer stacks of the Printed Wire Board (PWB) are used to reduce the coupling noise. The analog and digital signals in the circuit are clearly separated and shielded with analog ground and digital ground separately; the component layers (top and bottom layers) are separated from the noisy region (digital electronics) by a shield ground; the digital ground and analog ground are carefully designed to avoid any overlap; the power and ground planes for the front end ASICs are placed on many layers in order to reduce the path resistance. The assembled 96-pixel detector analog board is displayed in Figure 3.23 (b), which shows that the HERMES and SCEPTER chips are aligned close to the sensor in order to populate more chips conveniently around the sensor chip in case additional channels (such as 384) are required in the future. The buffer and differential driver for peak and timing detector are arranged close to SCEPTER dies to reduce the parasitic capacitance for high speed. Many capacitors are place in on the power rails of HERMES and SCEPTER to reduce the power supplies noise.

(a)



(b)

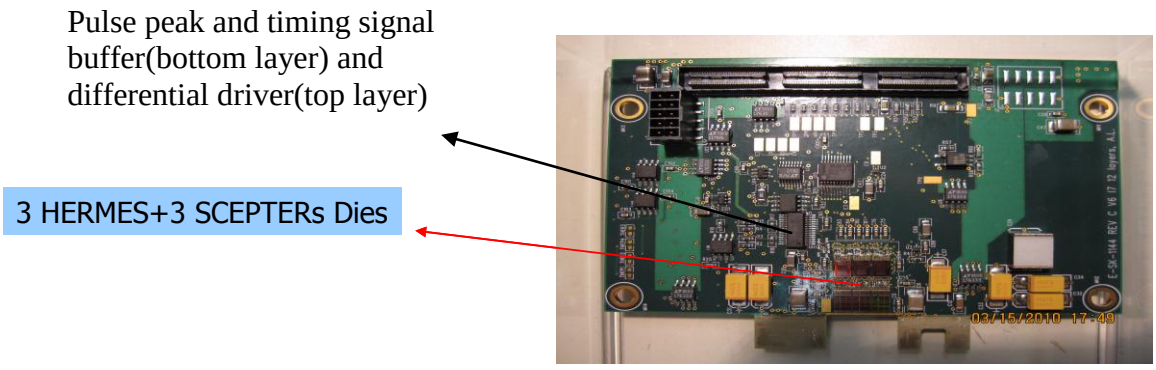


Figure 3.23 The 96-pixel detector analog board. (a) The block diagram. (b) The assembled board (96 pixel sensor is not mounted here).

3.3.3 Test

3.3.3.1 Board Design Verification Test

The verification test proceeded first to check the function of the board, followed by the detector characteristic test with a Fe^{55} source and synchrotron source at NSLS beamline X12A. Because of the new SCEPTER chip and added features, the firmware and application software of Maia system were changed. The design verification test was actually combined with hardware-software system integration tests of the Maia system.

In the function test, it was found that the SCEPTER threshold of discriminator varied with chips. This means that the threshold has to be adjusted from chip to chip to get the same energy range. Also, a 56 mV peak-peak noise was found on analog input of SCEPTER which is actually the coupling noise of the kick back of "Data Valid" signal of SCEPTER. It is reduced to 17mV peak-peak finally by adding extra conducting metal pieces to the ground planes of SCEPTERs to increase the thickness of ground planes; and a choke was added between the analog ground and digital ground planes to prevent the noise coupling. The board grounding system was enhanced further by increasing the thickness of the ground plane for HERMES chips; on the analog output of HERMES at 4 μs pulse shaping time a 3.7mV RMS noise level is achieved which is the low expected limit of the HERMES chip design. This concluded the best electronic noise level is reached with the new board. The test pulse shown in Figure 3.24, is a square wave generated by the DDM board and fed into the pre amplifier of HERMES chip where it is converted into Gaussian pulse output. It is for testing the function of the pulse processing and counting circuit. Since the Maia 96 board is designed with low noise technology, high energy resolution (<200 eV) is expected in the pulser test. The test pulses with

amplitude (v) of 0.037, 0.085, 0.218, 0.645, 0.818, 0.92, 1.02 are fed into HERMES chip, correspondingly the energy spectrums are collected in Figure 3.25(a) which shows energy pulse at the range of 339.6 to 3758 ADC channels (correspondingly representing the energy from 1,396.548 eV to 31,270.534 eV). The detector spectrum data is exported to the curve fitting tool, Figure 3.25(b) shows the curve fitting results. The corresponding energy resolution is calculated in Table 3.5. The results show that resolution of the circuit is independent of the energy and all of them are below 200 eV though in the actual case the resolution is proportional to the square root of energy, which is consistent with the Poisson distribution of photon created by electron and hole pairs in the photon diode.

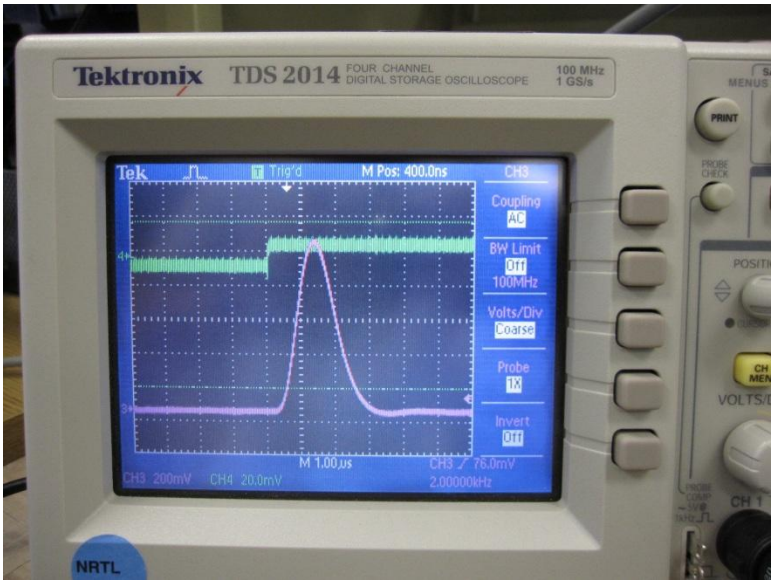
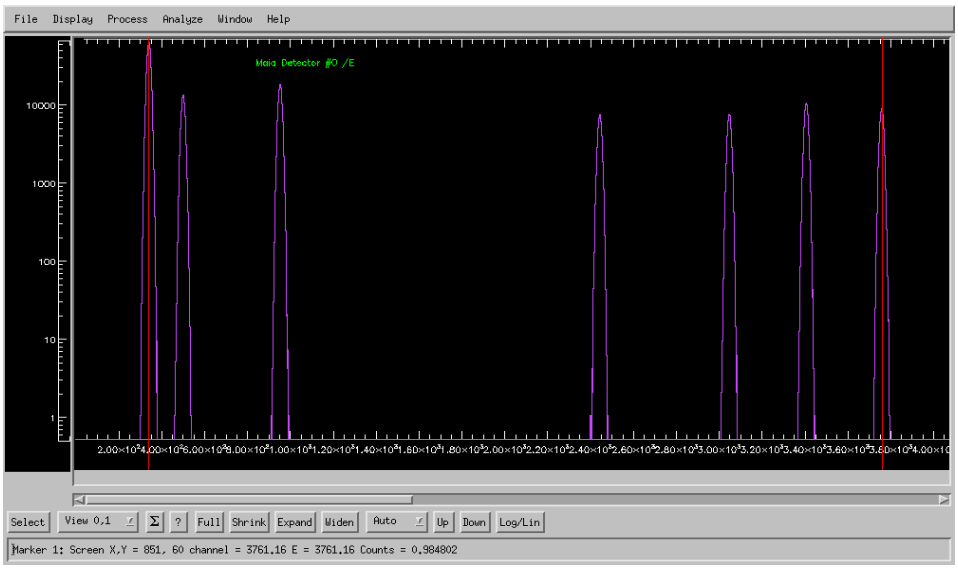


Figure 3.24 Square wave test pulse for calibration (channel 4) and its Gaussian pulse (channel 3) generated from the HERMES chip.

(a)



(b)

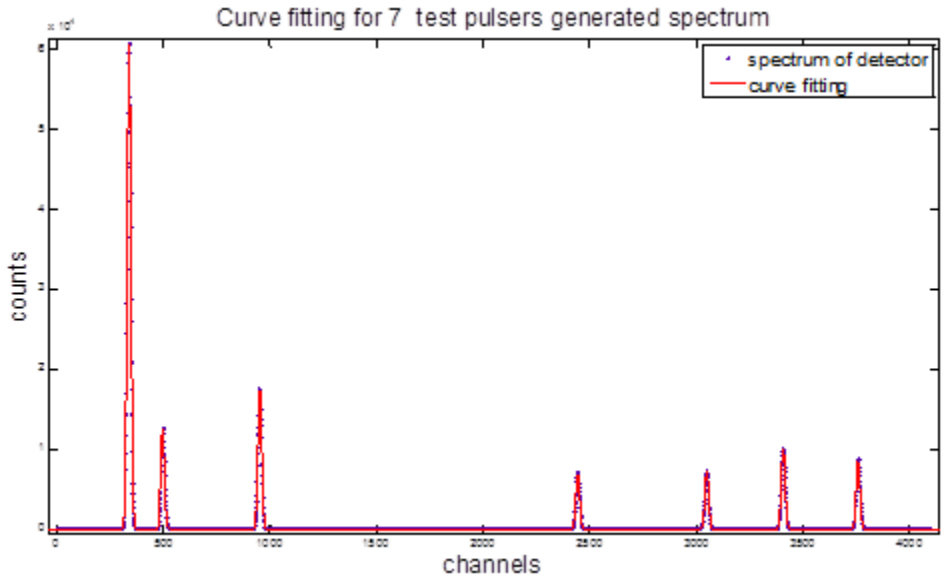


Figure 3.25 (a) Energy spectrum of the test pulse with amplitude (V) of 0.037, 0.085, 0.218, 0.645, 0.818, 0.92, 1.02. (b) Gaussian curve fitting for 7 test pulses generated spectrum.

Table 3.5 FWHM of Spectrum of 96-Element Maia Detector

Pulser	HERMES energy/pulse response				Spectrum	Gaussian fit				
Pulser Height (V)	energy (eV)	electrons	charge (C)	pulse (mV) (AC)	E (12-bit)	a	b	c	FWHM in ch	FWHM in eV
0.037	1,396.5	6.133E-17	9.83E-36	92	339.60	6E+04	339	12	20	176
0.085	2,732.3	1.200E-16	1.9236E-35	180	499.20	1E+04	499	12	20	177
0.218	6,679.1	2.933E-16	4.702E-35	440	951.90	1E+04	951	12	20	180
0.645	20,037.4	8.800E-16	1.410E-34	1320	2442.00	7052	2442	12	20	180
0.818	25,198.5	1.106E-15	1.773E-34	1660	3047.00	7331	**3047**	12	20	180
0.920	28,234.5	1.240E-15	1.987E-34	1860	3406.00	1E+04	3406	12	20	182
1.020	31,270.5	1.373E-15	2.201E-34	2060	3758.00	8708	3758	12	20	178

Another experimental test was to check the delay time between the PD/TD output of SCEPTER and ADC input to see if the Maia system can work with the 10 MHz readout clock. This measurement proceeded with a < 1pF probe and high speed oscilloscope to get the PD delay waveform. The first issue was that the DDM board could not provide clock rates higher than 6 MHz which is solved by the firmware change of DDM and finally it can go up to 15MHz. With the fastest device found on the market (AD8066 and EL5374), the delay of the analog output from the rise edge of readout clock is around 33ns, which is the concerned bottle net of speed of the entire system. This is displayed in Figure 3.26 where channel M1 is the analog output from differential driver; channel 4 is the “Data Valid” signal at the connector of DAM board; and channel 3 is the readout clock. The “Data Valid” circuit is another bottle neck that limits the speed of data collection because it has similar delay time with the analog signals. The latest high speed buffer and differential driver (EL5378) are intended to improve the analog signal time margin in the next assembly; the speed of “Data Valid” signal will be improved by adding a digital buffer between SCEPTER and FPGA. The second issue was that if the

clock rate is higher than 5 MHz, peak shifting in the spectrum occurs when DDM ADC starts the measurement. This might be due to the slow slew rate of “Data Valid” signal which caused the wrong triggering point of the high speed ADC when the “Data Valid” signal shows up behind the analog signals but this is not yet confirmed. A test module for this purpose was added in the firmware and it will be tested in future development. So far 5 MHz is good enough for the next step experiment.

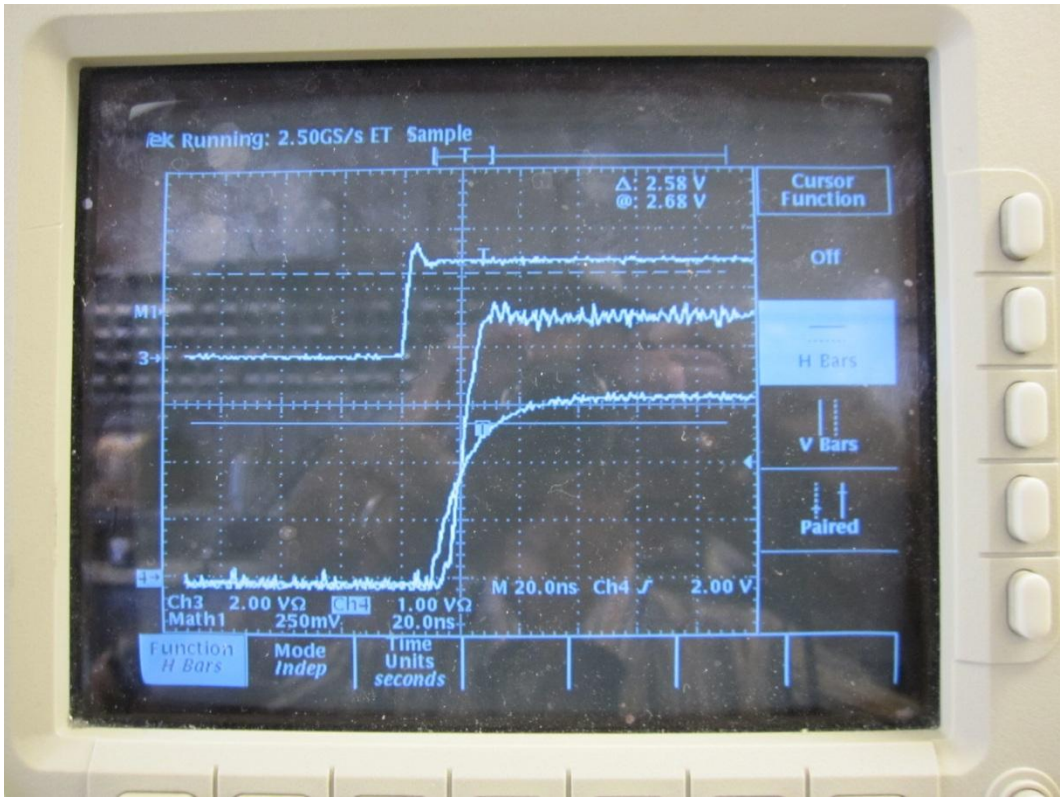


Figure 3.26 Timing measurement of PD path. Both channels M1 and 4 show the slow rise time, where channel M1 is the analog output after differential driver, channel 4 is the “Data Valid” signal, channel 3 is the readout clock.

A new GUI which is called “Maia control” was installed and tested with this DAM board. It can display the energy spectrum and time spectrum per single pixel or per group of pixels; also it has linearization and gain trim and pile up rejection features. With the “Maia control” program, the peak detector is observed to be spuriously triggered at

threshold energy instead of at the maximum amplitude when multiple channels of the same chip are pulsed at the same time. Also, the adjacent SCEPTER chip which has 7 channels pulsed at the same time could influence the channel under test. The latter problem was corrected by replacing the short wire with a ferrite bead between the analog ground and digital ground. An attempt was made to solve the first problem by adding more capacitors to filter the power supply noise and other potential noise sources. Unfortunately this did not help. Finally it was concluded that the problem can only be solved by redesign of the SCEPTER chip.

Another serious problem was that after power up the DAM board sometimes it works and sometimes doesn't, which means that if the "power enable" bit is set to 0 to turn off the power and then turn it on again by setting it to 1, the pre amplifier will not have the pulse output or the output produces very high noise. In another case, it will work fine if "power enable" is set to 1 before the power cycle proceeded. The power up timing was checked and it is found that the DDM refreshes the DAM registers 0.5 s after the "power enable" bit is set, but the regulators on DAM board can't provide full power until 4 s of delay; such an example is displayed in Figure 3.27, which shows the register refresh process starts 0.5 s after "auto power on" bit is set but the power of SCEPTER only comes to full power after 4 s. Hence the registers of DAM are not properly configured and consequently the dies work unexpectedly. The problem was finally fixed by changing the firmware of DDM to delay register refreshing for 5 s after "power enable" bit is set.

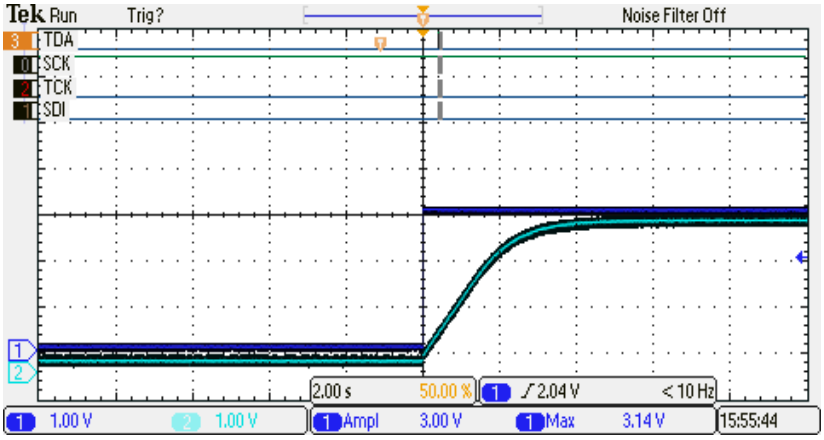


Figure 3.27 Power up timing. TDA, SCK, TCK, SDI are the SPI signals to configure the registers. Channel 1 is the "auto power on" control bit to power up the DAM. Channel 2 is the power supplies output for SCEPTER dies.

To conclude the function verification test, the Maia 96 board was successfully developed. The system shows the expected energy resolution from 1 keV to 33 keV energy detection range with pulser, which is less than 183 eV. The test set up is displayed in Figure 3.28 where the DAM board is on the left side of picture; DDM is on the right side; fiber to the HYMOD is the yellow color cable. There are two issues remaining for the future development. First, the Maia system can get the wrong reading when the readout clock is higher than 5 MHz. This is caused by both the slow skew rate of the "Data Valid" signal and analog signals. Second, SCEPTER will have "low energy events" when multiple channels are pulsed at same time. SCEPTER needs to be redesigned to fix this problem.

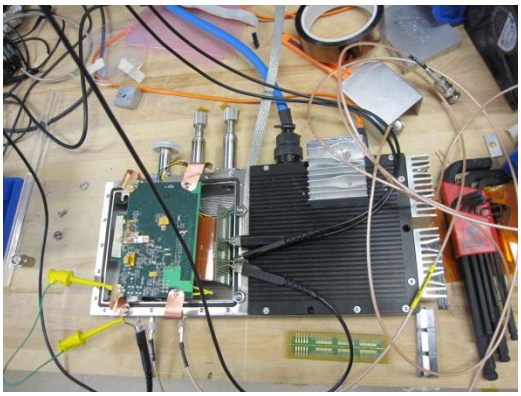


Figure 3.28 Maia 96-element detector board in the test.

The 96 channel detector array is bonded on the DAM board later. Several thermistors are added to monitor the temperature changes of the HERMES chip, the sensor, and the cooling water. Figure 3.29 displays the metal housing with cooling system. Figure 3.30 (a) and (b) show the whole assembly. The sensor chip is glued onto two Peltiers (8W/each). The Peltiers are glued onto the water cooling metal pieces. The 150 V bias is applied to the aluminum plane of sensor which connects with the N+ side of photo diode by a blue wire. Figure 3.31 displays the whole detector system which includes the Maia control system, the GUI, DAM box, DDM box, fiber and HYMOD shelf.

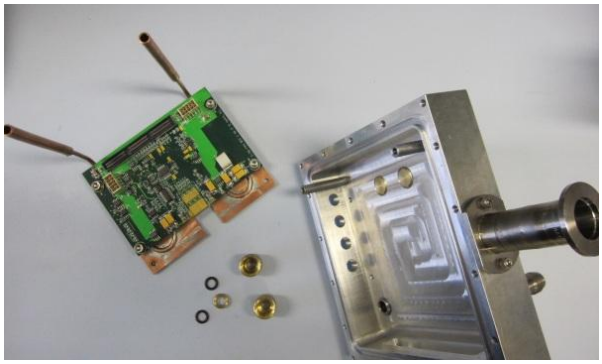


Figure 3.29 The 96-element detector metal housing and cooling system.

(a) (b)

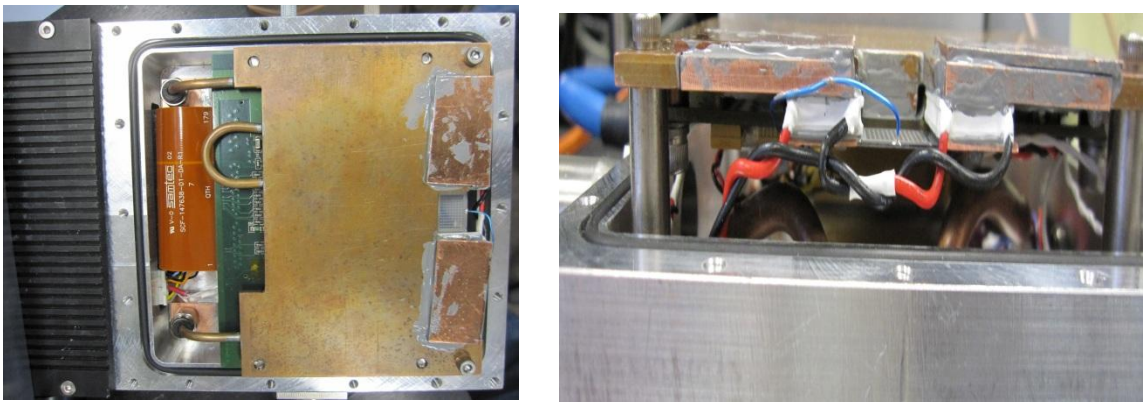


Figure 3.30 The 96-element detector module. (a) Entire assembly. (b) Side view of sensor assembly; the sensor is glued onto two peltiers (white); peltiers are glued onto the water cooling metals. Blue wire is for 150 V bias. Red and Black wires is for pelters power (4 A).

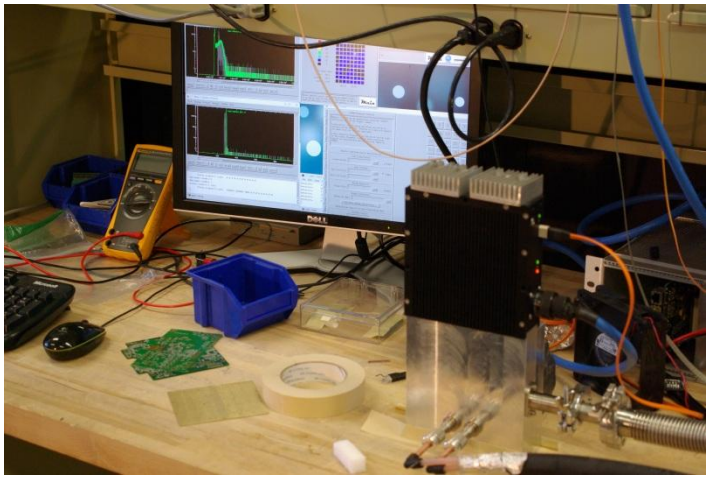


Figure 3.31 Maia 96-element detector system including PC, DAM, DDM, fiber and HYMOD.

3.3.3.2 Test with Radiation Sources

The Energy spectrum and its corresponding pulse timing spectrum (time over threshold) of Fe^{55} are acquired with the new detector in Figure 3.32. The detector configuration for this data acquiring is as follows:

Bias: 150V

Leakage: changes between 0.000 and 0.01 μA

Detector temp: -25º C

Water temp: 11.8º C

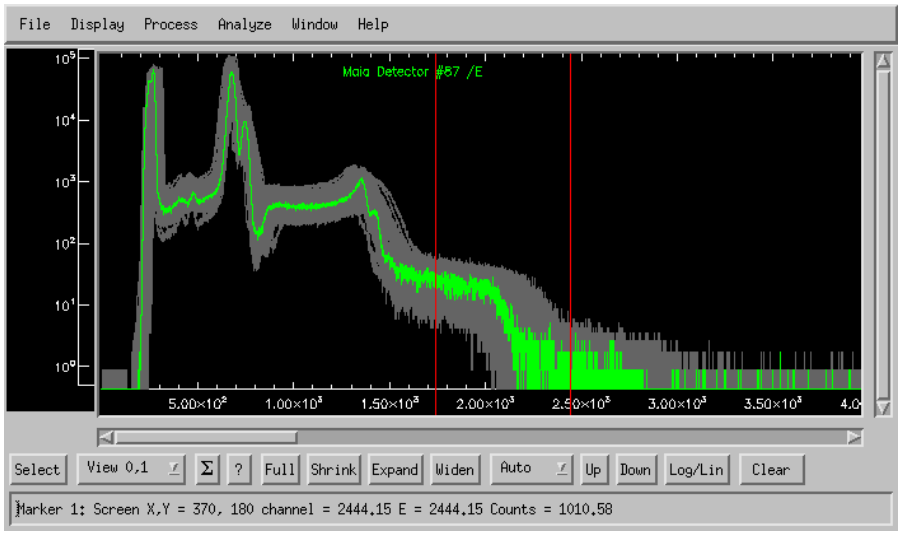
Timing mode: time over thresh

Gain: 1500mV/fC

Shaping time: 4.0 μs

One can notice that there is a big peak at low energy in Figure 3.32, which was called "odd/even" events (by scientists in Australia) for the reason that it most likely happens on either even or odd channels, exclusively, and was also called the "low E" event mentioned early. The PD of SCEPTER is triggered at threshold level instead of the maximum level for unknown reasons when the multi-channels are active to collect the photons. The photon pulse is consequently wrongly captured and displayed in the energy spectrum as the spike in the low energy region. In order to reach the lower minimum detectable energy for detector use, the spike can be moved outside the region of interest by adjusting the threshold voltage for each detector element. The only problem left is the counts lost because of registering the wrong energy.

(a)



(b)

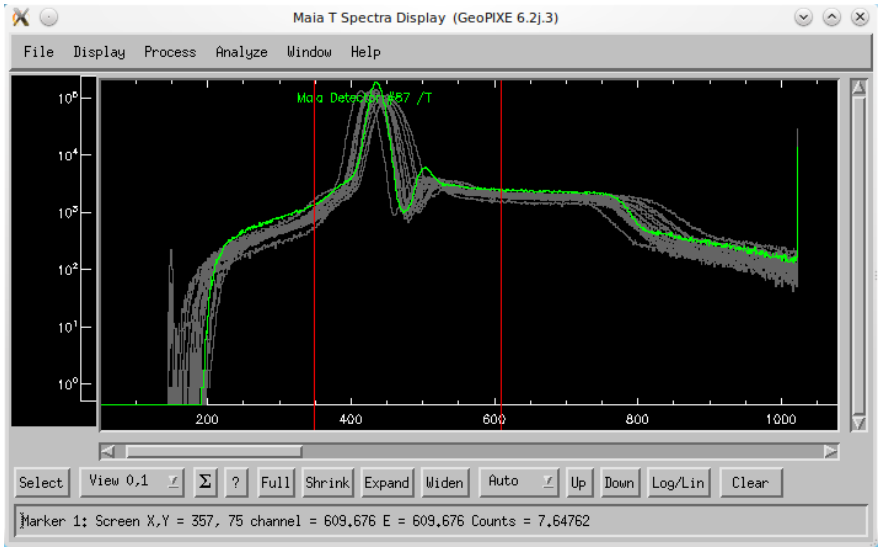
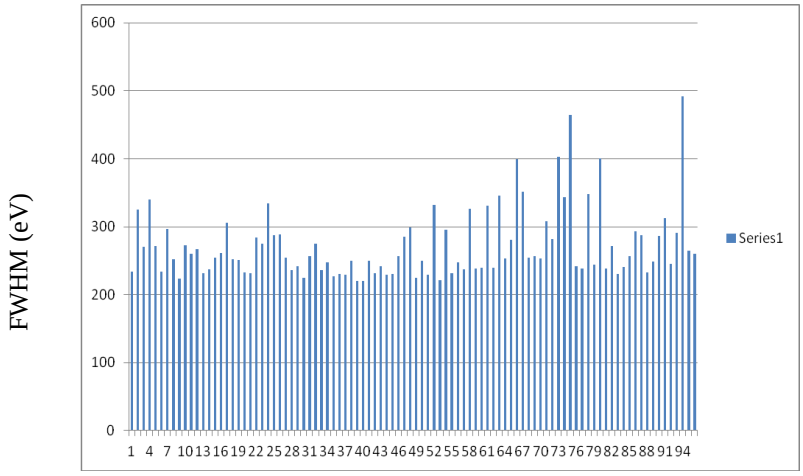


Figure 3.32 (a) Fe^{55} energy spectrum for 96 detectors. Mn K_α and K_β peaks could be easily identified. (b) Time over threshold spectrum of pulses in (a).

Figure 3.33 displays the FWHM (Mn K_α peak) of 96 channels for 4 μs shaping time at 5k counts/s rate, it shows that the best FWHM is 230 eV and a majority of the detector elements (pixels) are below 260 eV.

(a)



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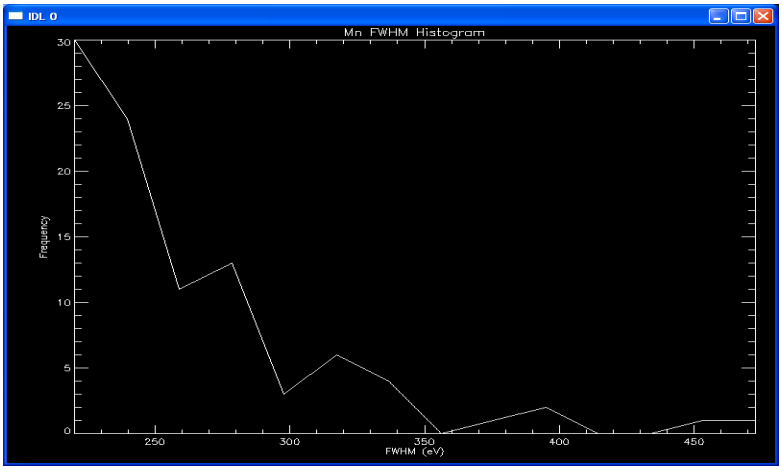


Figure 3.33 FWHM (Mn K_α peak) of all 96 channels for 4 μs shaping time at 5k counts/s rate. (a) FWHM vs. channel number. (b) FWHM histogram with 20 eV bins.

3.3.3.3 Test with Synchrotron Source

The detector characteristic tests at high flux were conducted at NSLS beamline X12A, at BNL. FWHM vs. counting rates at different shaping times, intensity linearity and energy response linearity were checked. Energy calibration was performed with a broad range of different standard foils. Finally, a dust sample is tested and analyzed to see what elements are contained for a real world sample with low metal content; EXAFS measurements were conducted on a UO_2 single crystal sample at U L3 edge. The set up for the test is

displayed in Figure 3.34 (a), where the incident beam is incident from the left side. Note that the incident beam direction is parallel to the detector window while the sample plate is tilted with 45 degree to the beam direction to reduce the intensity of elastic scattering directly into the detector window. The detector window has ¼ mm thickness beryllium which attenuates beam intensity. According to $I = I_0 e^{-\mu t}$ where I is the transmitted X-ray intensity, I_0 is the incident X-ray intensity, μ is the absorption coefficient, t is the thickness of sample. I/I_0 vs. Energy (100 eV to 10 keV) is plotted in Figure 3.34 (b) which shows that the transmitted X-ray intensity is less than 50% if the sample fluorescence energy is lower than 3 keV.

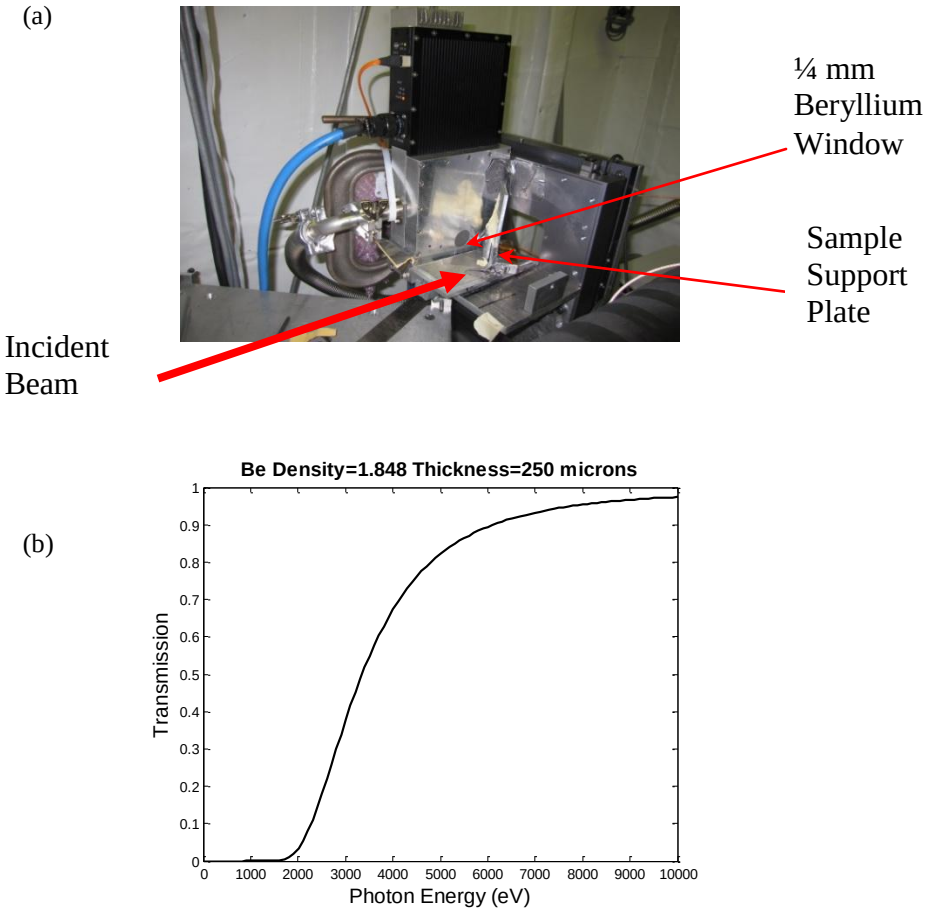
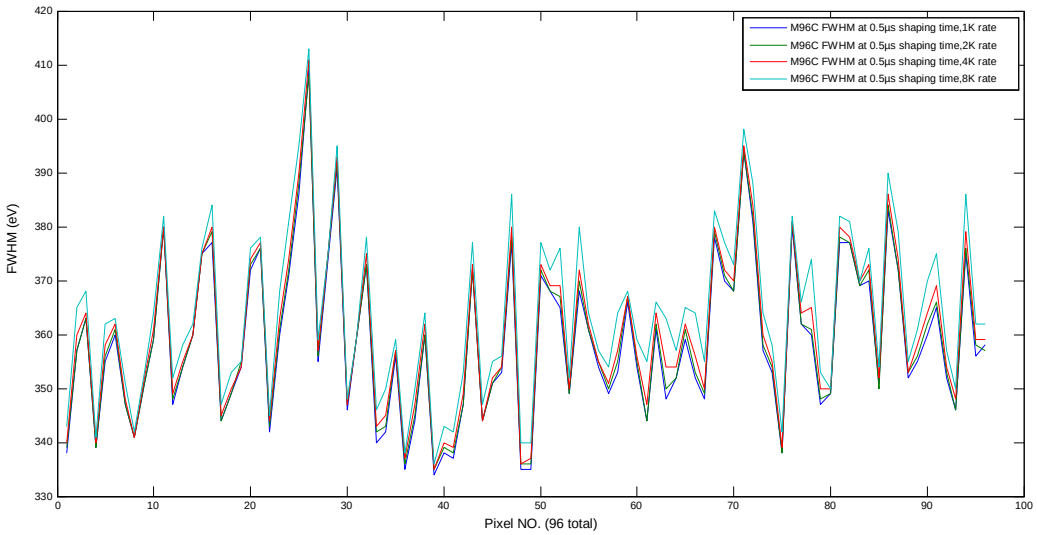


Figure 3.34 (a) Test set up at beamline X12A, BNL. (b) Transmission vs. photon energy for the ¼ mm Be detector window [28].

(a)



(b)

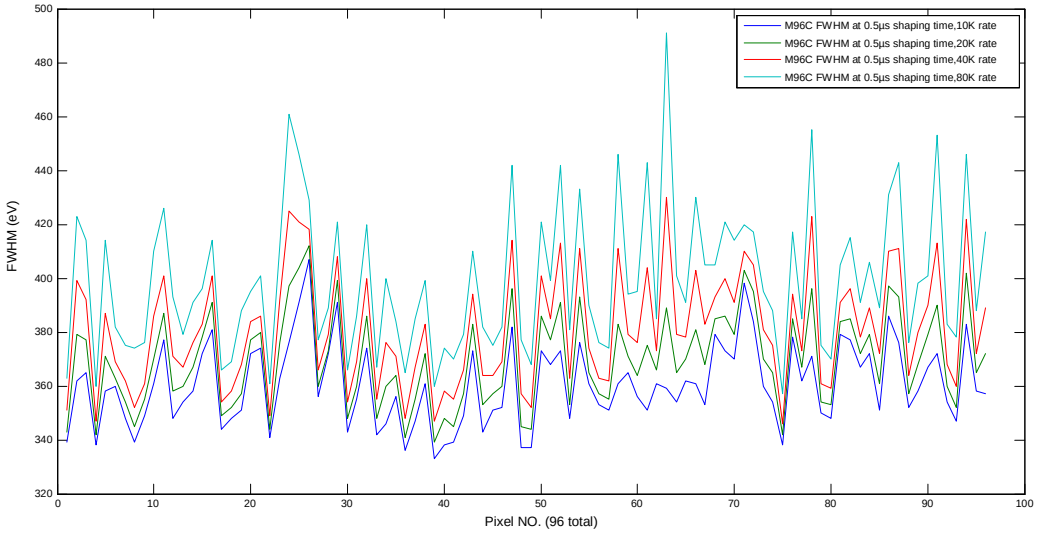
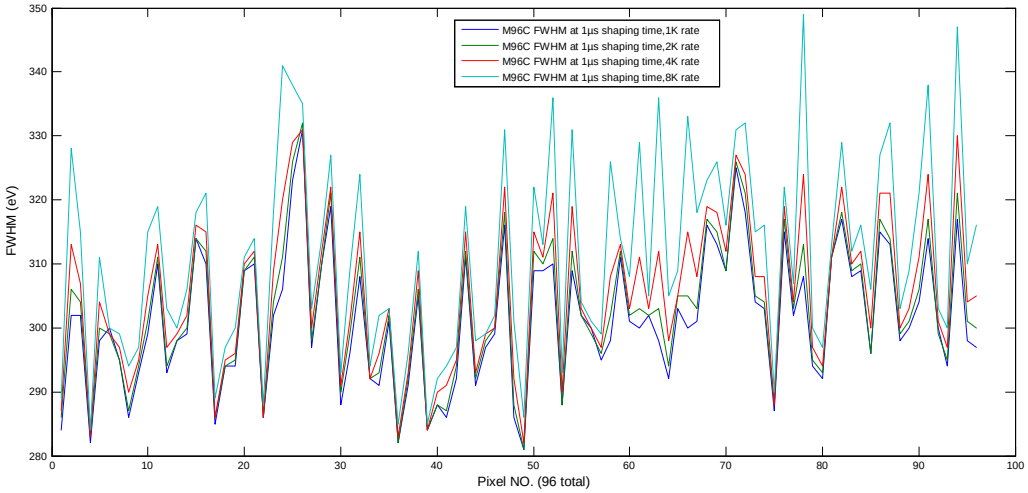


Figure 3.35 FWHM of all 96 pixels at 0.5 μs shaping time at different counting rates. (a) At 1k, 2k, 4k, 8k counts/s. (b) At 10k, 20k, 40k, 80k counts/s. Here and below these rates are the total output counting rates registered by the detector.

(a)



(b)

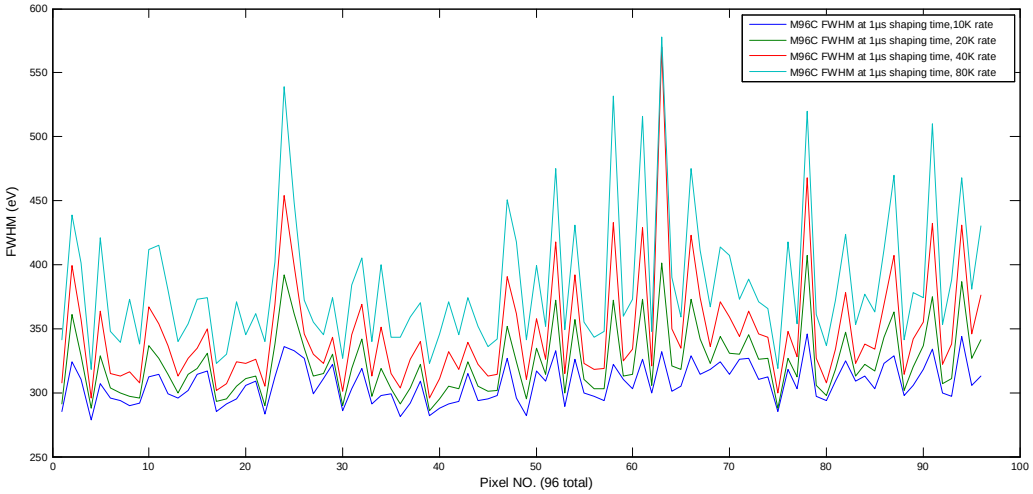
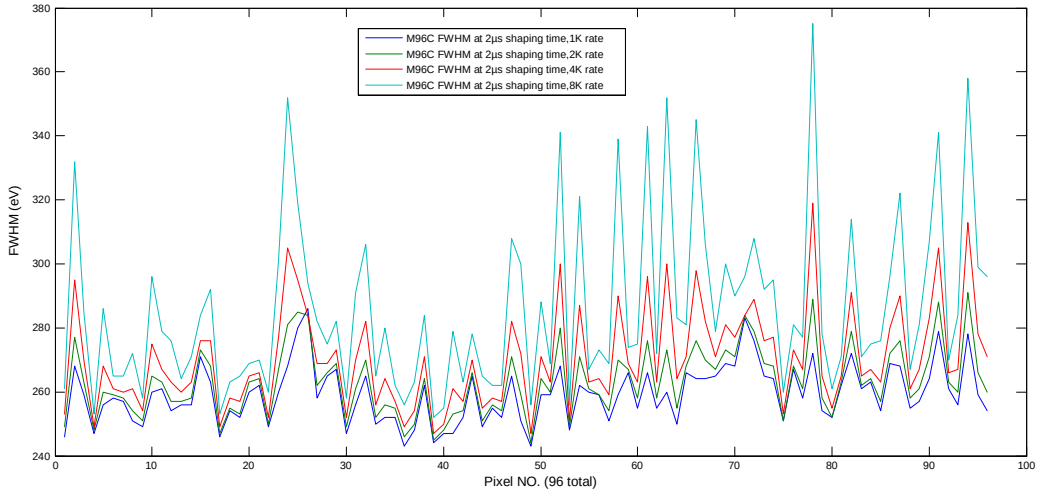


Figure 3.36 FWHM of 96 pixels at 1 μs at different counting rates. (a) At 1k, 2k, 4k, 8k counts/s. (b) At 10k, 20k, 40k, 80k counts/s.

(a)



(b)

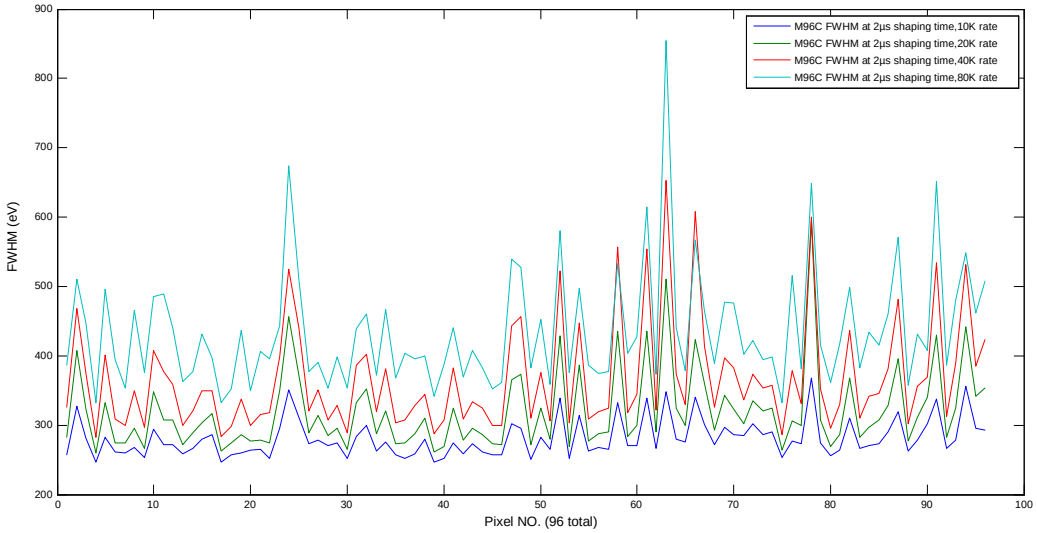
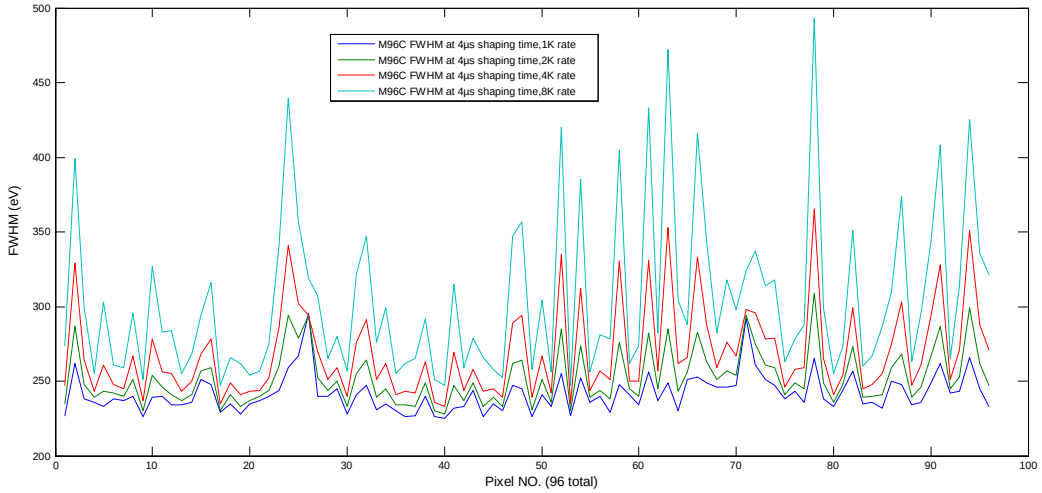


Figure 3.37 FWHM of 96 pixels at 2 μs at different counting rates. (a) At 1k, 2k, 4k, 8k counts/s. (b) At 10k, 20k, 40k, 80k counts/s.

(a)



(b)

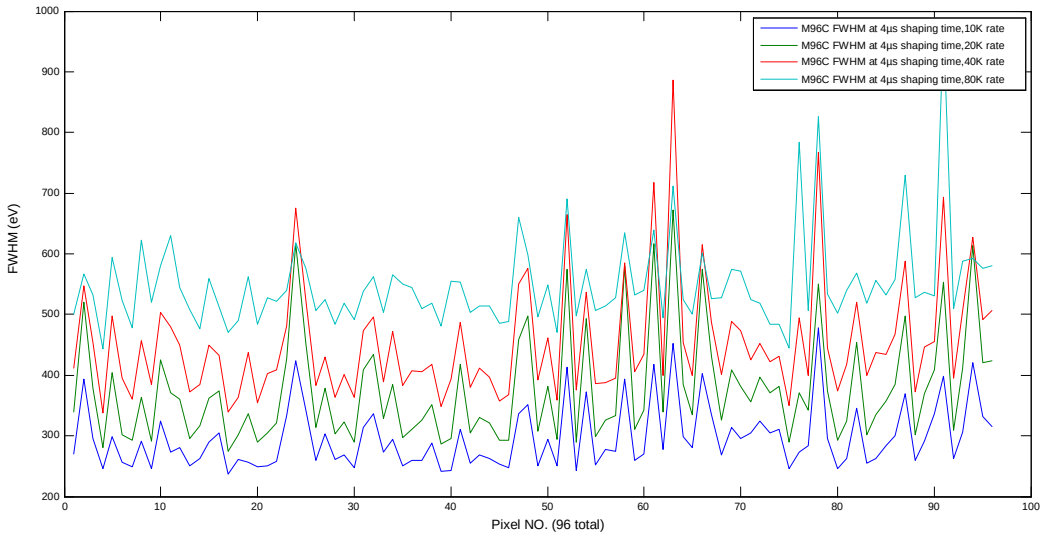


Figure 3.38 FWHM of 96 pixels at 4 μs at different counting rates. (a) At 1k, 2k, 4k, 8k counts/s. (b) At 10k, 20k, 40k, 80k counts/s.

Figure 35 to Figure 38 show the FWHM of all 96 pixels for the Co K_α peak when the incident photon flux is changed to make the output counting rate vary from 1k to 80k counts per second. The pulse shaping time is set to 0.5 μs, 1 μs, 2 μs, or 4 μs respectively. It shows that the FWHM is degraded if the counting rate is increased. This

is demonstrated clearly in Figure 3.39 where channel 22 is plotted as an example. The 1 μs shaping time pulse has the best energy resolution if moderate high counting rates is required (30k counts/sec). On the other hand, 2 μs shaping time is best if low counting rates are required. For high counting rates (80k counts/sec) and stable resolution for the full intensity range (~350 eV), a shaping time of 0.5 μs should be used. For the full detector array this give a total counting rate of more than 8 MHz.

The results found corresponding to the expectation of the low noise design of HERMES, where the noise depends on the shaping time and total input capacitance of shaper circuit. If the input capacitance is fixed, the bigger the shaping time, the smaller the noise. If the shaping time is fixed, the bigger the input capacitance, the bigger the KTC white thermal noise on the capacitor. Therefore, at low counting rate, the best resolution is at a shaping time of 2 μs. At high counting rate, the pile-up events will destroy the energy resolution for slower pulses (bigger shaping time), that is why the energy resolution for 2 μs shaping time degrades faster than for 1 μs in Figure 3.39.

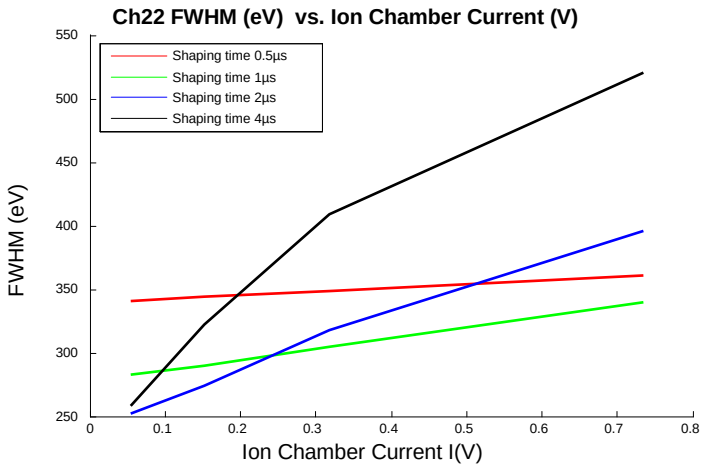


Figure 3.39 FWHM of channel (CH) 22 at different shaping times and different incident beam flux in the units of voltage, which is corresponding to rates from 10k counts/s to 80k counts/s.

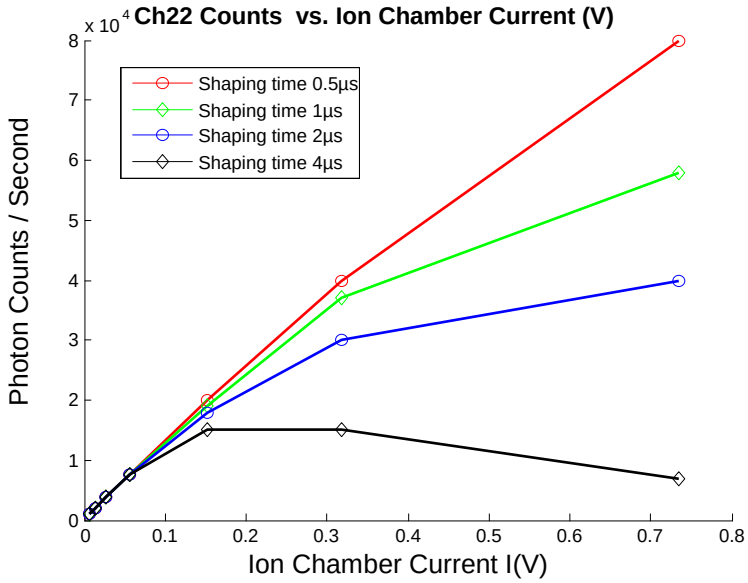


Figure 3.40 Channel 22 counting rate vs. Ion chamber current when all pixels are enabled and shaping time is varied (the 7 data points correspond to 1k, 2k, 4k, 8k, 20k, 40k, 80k counts/s in detector output).

The intensity linearity of detector is related to the dead time, which is the finite time required by the detector to process an event [16], the sensor array and pre-amplifier are sensitive to the photon events during the dead time. Admittedly the pile-up will happen if other events arrive during the dead time and the dead time will be prolonged, which is called extendable dead time. On the other side, the SCEPTER has only 8 peak detectors for 32 channels and it is insensitive to other events during dead time if it is locked for an event. This affects the observed counting rate. From Figure 3.40, it shows that when incident photon intensity is increased, the linearity is not maintained when all pixels are enabled. As noted, measurements for 0.5 µs shaping time are roughly linear up to 80k counts/s (40k counts/s for the more linear 5% bending point), the experiment also shows that the maximum counting rate per pixels is ~110k counts/s at 5MHz read request clock rate. The 1 µs shaping time curve starts to bend at around 35k counts/s, the 2 µs

shaping time curve starts to bend at around 20k counts/s and 4 μs shaping time curve starts to bend at around 10k counts/s. The detector registered counts are proportional to mT*exp(-mτ/n) where m is the true counts, T is the time period to observe the detector registered counts, τ is the shaping time, n is a factor of ~10%. It can be seen from the figure that the 4 μs shaping time curve saturates at the point of n/τ (~20k counts/s).

For energy calibration, the energy responses of different samples are measured. Figure 3.41 displayed the accumulated emission lines of sample Zr, Se, Cu, Mn, Ca and S in the detector spectrum of pixel 22, where the horizontal axis is the ADC channels (Total =4096 channels for energy axis), the vertical axis is the photon counts accumulated. Figure 3.42 displays the accumulated emission lines of sample Ge, Cu, Co, Ti and Cl. Table 3.6 lists the emission line energies and ADC channels reading from detector of these samples. Displayed in Figure 3.43, the linear fit result for the curve is that the Energy (eV) = 8.3753* ADC channels-654.57; it is observed that it is almost linear except the high energy portion which is a little bit off from the fitted linear curve. It is conclude that the detector performs as expected.

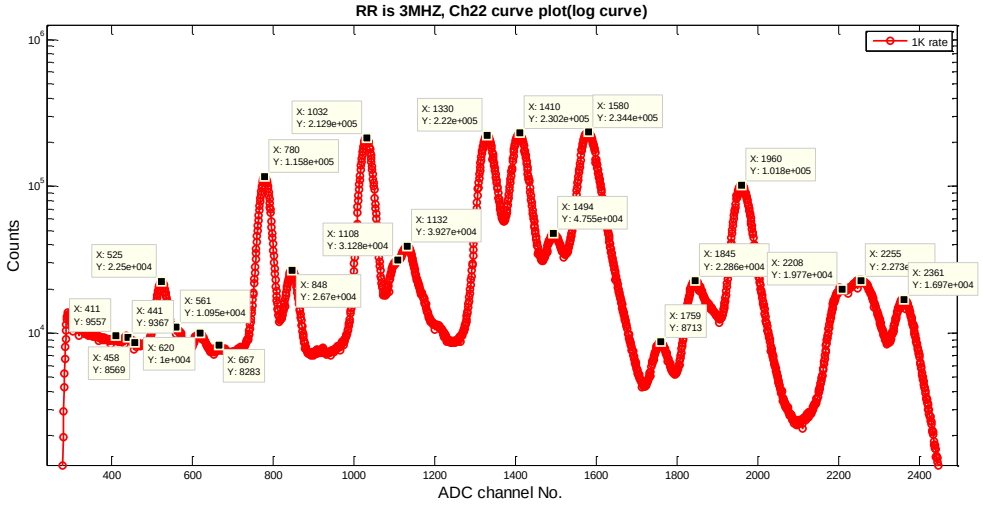


Figure 3.41 Accumulated emission lines of Zr, Se, Cu, Mn, Ca, S samples on channel 22. The Incident photon energy was 21 keV.

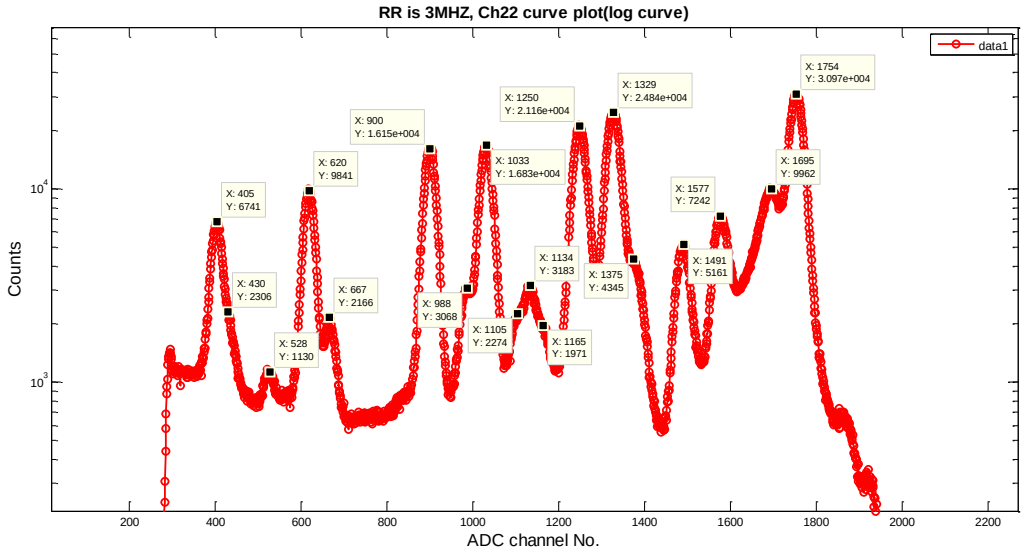


Figure 3.42 Accumulated emission lines of Ge, Cu, Co, Ti, Cl samples on channel 22.

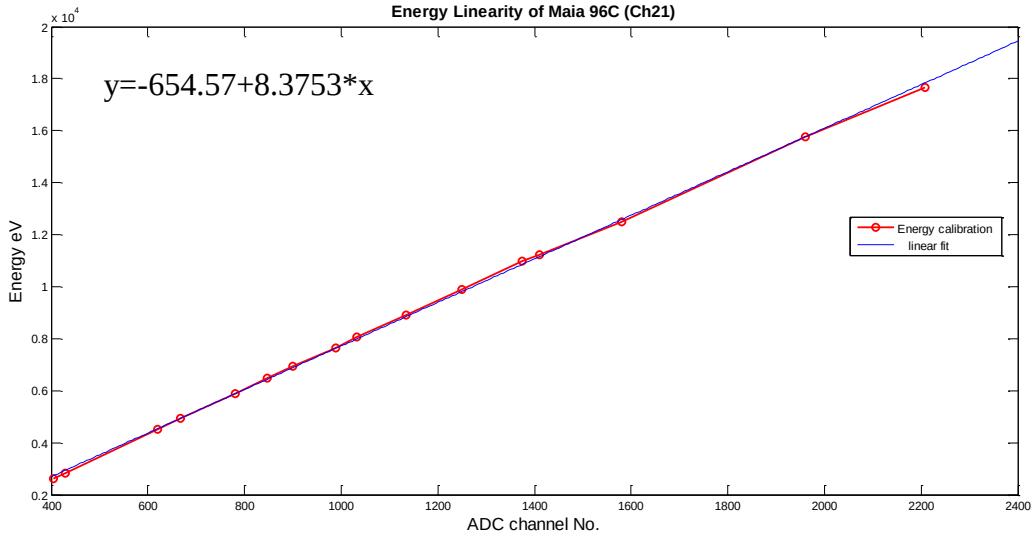


Figure 3.43 Emission line Energy vs. ADC channels of detector for prominent peaks of Cl, Ti, Mn, Co, Cu, Ge, Se, Zr. Note that the curve it is almost linear and the Energy (eV) is equal to 8.3753 * ADC channel number - 654.57.

Table 3.6 Energies and the Corresponding ADC Channels of Emission Lines of Cl, Ti, Mn, Co, Cu, Ge, Se, Zr

ADC channel	405	430	620	667	780	848	900	988
Energy (eV)	2622	2816	4510	4931	5899	6490	6930	7649
Element	Cl K_α	Cl K_β	Ti K_α	Ti K_β	Mn K_α	Mn K_β	Co K_α	Co K_β

ADC channel	1033	1134	1250	1375	1410	1580	1960	2208
Energy (eV)	8048	8905	9886	10982	11224	12496	15775	17668
Element	Cu K_α	Cu K_β	Ge K_α	Ge K_β	Se K_α	Se K_β	Zr K_α	Zr K_β

The low and high detectable energy range with Cl and UO_2 samples are explored. Pixel 44 is selected and Fe^{55} source is used for the low detectable energy test (beamline is closed at the time). First a plastic sample container is measured. The spectrum is displayed in Figure 3.44, where the emission lines of Al, Si escape are from detector itself; Mn lines are from Fe^{55}; and the Ar which is from the air. The salt (NaCl sample) is attached on the plastic box for the fluorescence experiment and Cl K_α peak is clearly seen in Figure 3.45. The Al K_α peak is observed in both cases. Table 3.7 lists the emission line energies and the corresponding ADC channel reading obtained from the detector for the test. Figure 3.46 displays the spectrum of UO_2 and Table 3.8 lists the emission line energies and the corresponding ADC channel reading for this sample. It shows that Uranium (U) $L_{\alpha 1}$, $L_{\beta 1}$, $L_{\beta 2}$, $L_{\gamma 1}$ can be seen.

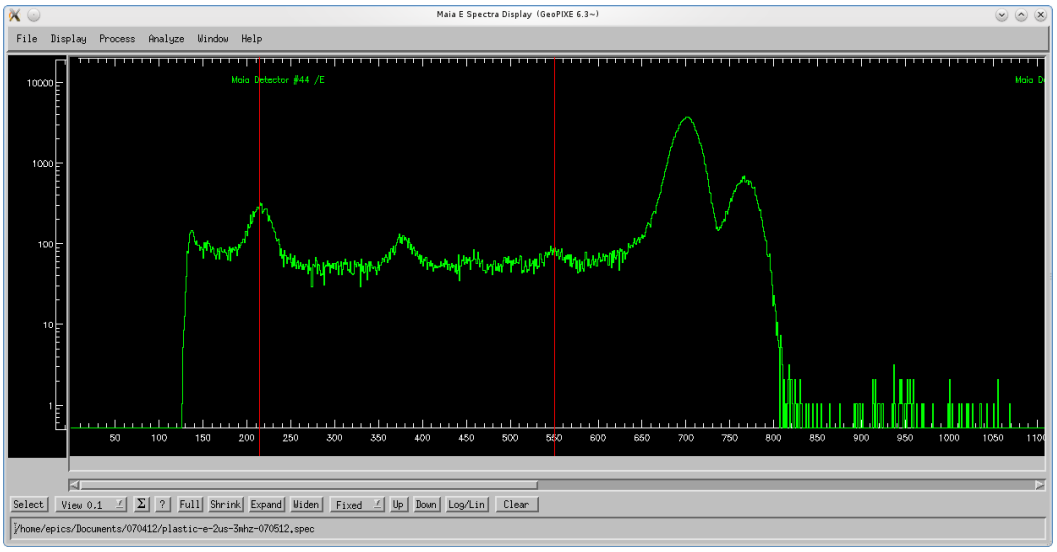


Figure 3.44 Spectrum of the plastic container on pixel 44 (Fe^{55} source), the peaks positions (ADC channel number) are 217 (Al), 377 (Ar), 550 (Si esc.), 701 (Mn K_α), 770 (Mn K_β).

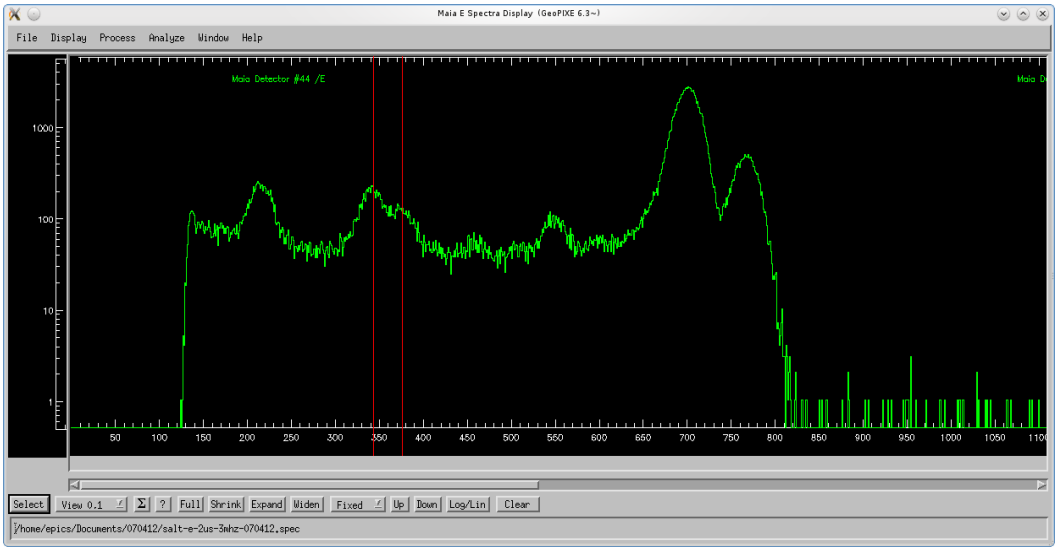


Figure 3.45 Spectrum of the Cl placed on plastic box on pixel 44 (Fe^{55} source), the peaks positions are 217(AL), 345(Cl K_α), 377(Ar), 550(Si esc.), 701(Mn K_α), 770(Mn K_β).

Table 3.7 Energies and the Corresponding ADC Channels of Emission Lines of Cl, Al, etc.

ADC channel	217	345	377	550	701	770
Energy (eV)	1486	2622	2957	4158	5899	6490
Element	Al K_α	Cl K_α	Ar K_α	Si esc.	Mn K_α	Mn K_β

Table 3.8 Energies and the corresponding ADC channels of Emission Lines of UO_2, Cu

ADC channel	1035	1139	1335	1499	1587
Energy eV	8044	8917.6	10564	11941.6	12680.8
Element	Cu k $_\alpha$	Cu K $_\beta$			

ADC channel	1709	1857	1979	2062	2136	2263	2384
Energy eV	13705.6	14948.8	16670.8	17292.4	18359.2	19375.6	19938.24
Element	U L $_{\alpha 1}$	U L $_{\alpha 1}$		U L $_{\beta 1}$			U L $_{\gamma 1}$

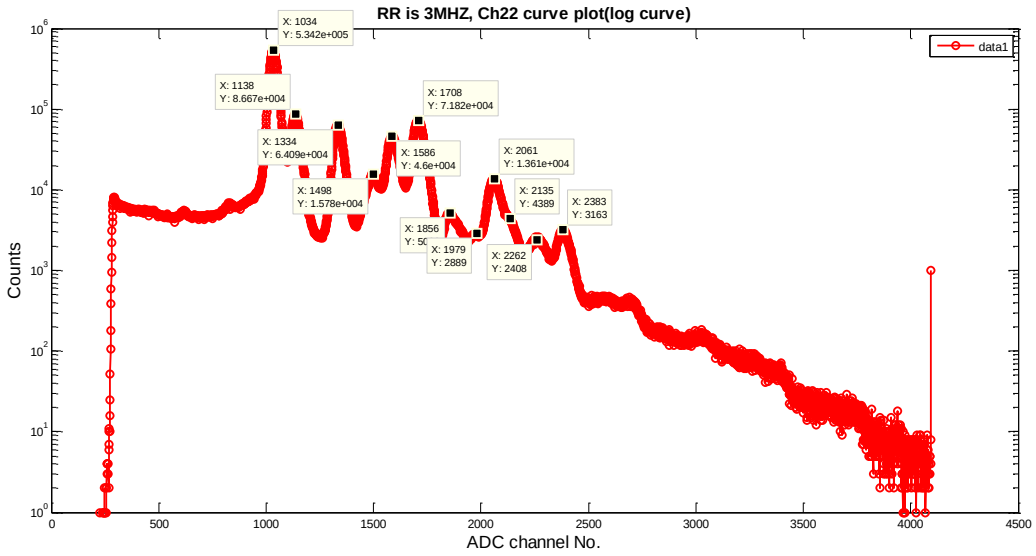
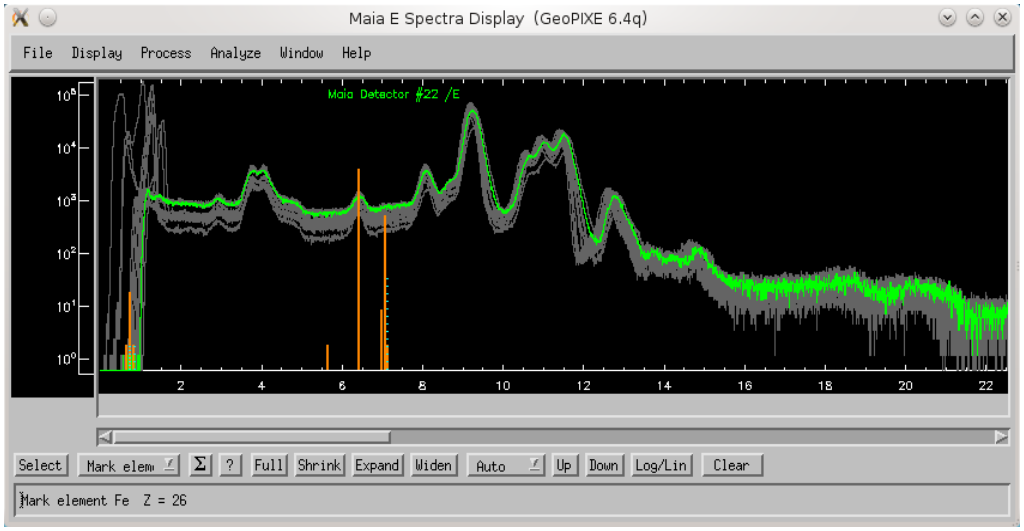


Figure 3.46 UO_2 fluorescence spectrum displayed on pixel 22 of detector. The incident photon energy is 21 keV.

The Maia functions of linearization, gain trim, X-ray energy calibration, pile-up rejection, group spectrum were verified. Procedures to set up the Maia system with linearization and gain trim can be found in Appendix A. The linearization function adjusts the energy response of each pixel with test pulses of different amplitudes which represent different energies. The gain trim alignes the peaks of the spectrum of each pixel. The X-ray energy calibration converts the ADC channel number to real energy. The pile-up rejection rejects the counts for pile-up events. The group spectrum is the summation of spectra over a group of pixels which can be defined by the user. A sample of $Fe_{0.06}IrTe_2$ was used to test these functions. The incident energy of beam is 11.4 keV which is above Ir L3 absorption edge (11.215 keV). Figure 3.47 and Figure 3.48 display the spectrum of the sample, which is linearized, gain trimmed, X-ray energy calibrated. The spectrum of channels shows that they are peak aligned, the counts are displayed vs. real energies instead of ADC channels, the Fe, Ir, Te emission lines are displayed in Figure 3.47 (a), Figure 3.47 (b) and Figure 3.48 (a). Figure 3.48 (b) shows the comparison of group (all 96 pixels with 3 disabled) spectra and the single pixel spectrum (Channel 10). With pile-up rejection, the group spectrum doesn't show the high spike in the low energy region, which is caused by the low energy event of SCEPTER. Also, the high energy peaks become more obvious.

(a)



(b)

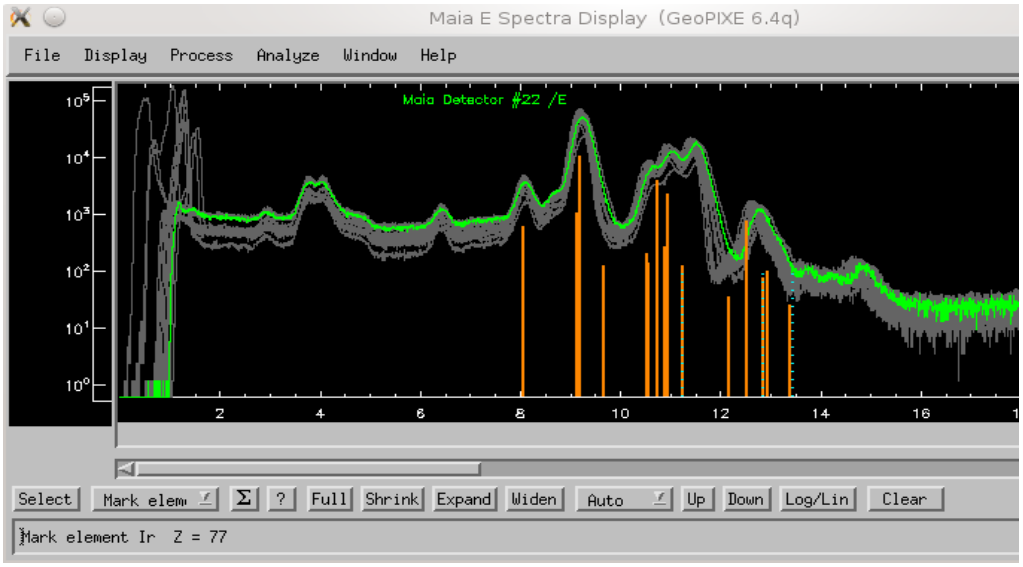
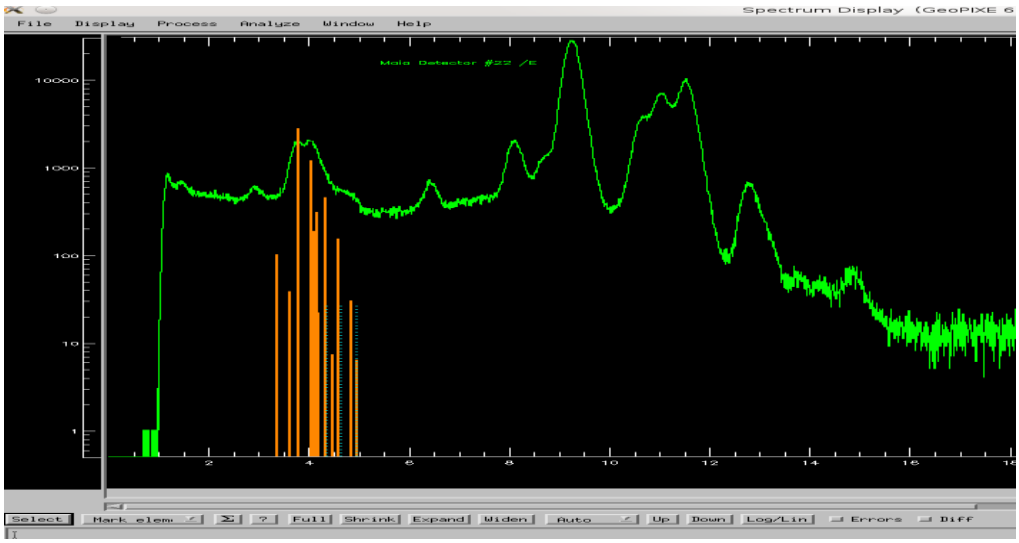


Figure 3.47 Energy calibrated spectrum of $Fe_{0.06}IrTe_2$. The incident photon energy is 21 keV. (a) Spectrum with tabulated Fe emission lines. (b) Spectrum with tabulated Ir emission lines.

(a)



(b)

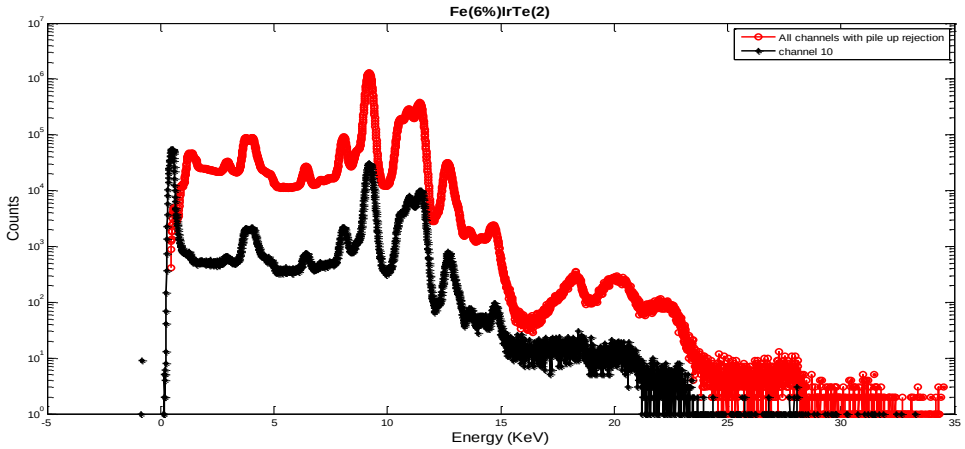
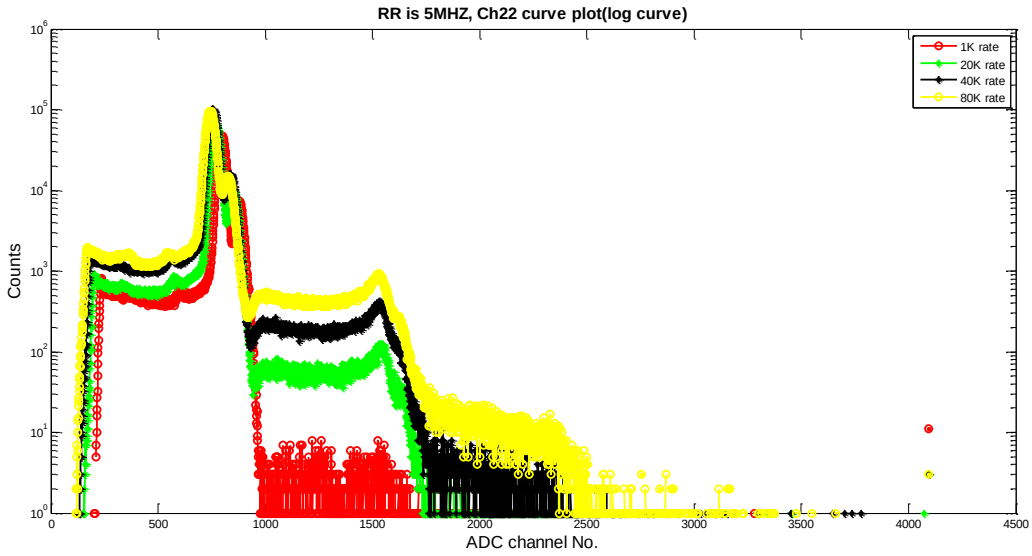


Figure 3.48 Energy calibrated spectrum of $Fe_{0.06}IrTe_2$. The incident photon energy is 21 keV. (a) Spectrum with tabulated Te emission lines. (b) Comparison of group (all 96 pixels with 3 disabled) spectrum and signal pixel spectrum (Channel 10). With pile-up rejection, the group spectrum does not show the high spike in the low energy region, which is caused by the low energy event of SCEPTER. Also, the peaks at high energy become more obvious.

In the experiment with Co foil, it was found that either the fluorescence energy or time (time over threshold) peaks of Co shifted if the incident photon intensity is changed. As displayed in Figure 3.49, when the Read Request clock (RR) is 3 MHz, shaping time is 0.5 μs and incident photon counts is changed from 1k to 20k, 40k, 80k counts/s, the whole energy spectrum shift backward around -52 ADC channels (corresponding to 52*0.5V). It was found that the problem is related to the pulse activities on PD/TD output, the peak shift problem was simulated with a radioactive source (Fe^{55}) where the counting rate of incident photon is fixed at 1k counts/s and the RR clock rate is 100k Hz. The peak shift is about 60 ADC channels from the spectrum when all pixels are active and lots of events appear on PD/TD outputs to the spectrum when only one pixel is active and few events appear. This is the worst case of the peak shift observed in the detector when the counting rate is changed. The baseline bias points were checked at both ADC and differential driver and a ~30mV shift was observed on the baseline at the differential driver. The 1.5v/1.0v bias circuit was suspected to be wrong and 2V, 100k Hz with 50% duty and certain offset was applied to the PD output of SCEPTER. A ~45 mV shift is observed on INN pin of EL5374. The problem was caused by the resistor R1 in Figure 3.50 (a) which is 10k ohm, Figure 3.50 (b) shows that with such a big resistor, the shift is about 45mV from the Pspice simulation if 100k Hz stimulus is added. If R1 is changed to 50ohm, the peak shift is +5 ADC channels only when rate is changed from 1k counts/s to 80k counts/s when RR is 3MHz with 0.5 μs shaping time. The R1 resister value was changed and detector was put back into test, the Co K_α peak positions (ADC channels) at different rates were: 863 at 1k rate (Ion chamber I=0.0067V), 864 at 20k rate (Ion chamber I=0.1521V), 865 at 40k rate (Ion chamber I=0.3186V), 868 at 80k rate (Ion

chamber I=0.7356V), which are displayed in Figure 3.51. It is concluded that the peak shift problem is fixed when R1 is changed to any value from 0 to 50 ohm.

(a)



(b)

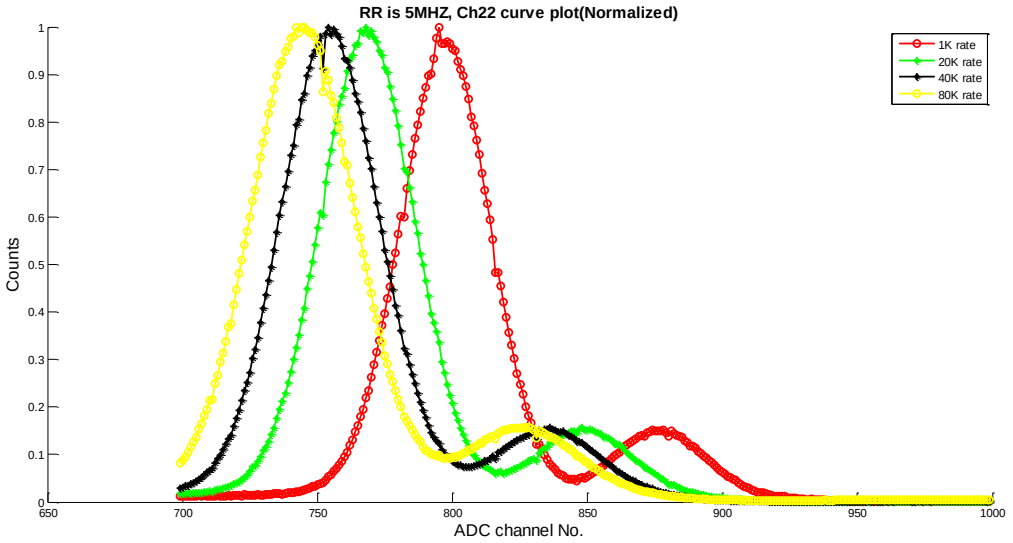
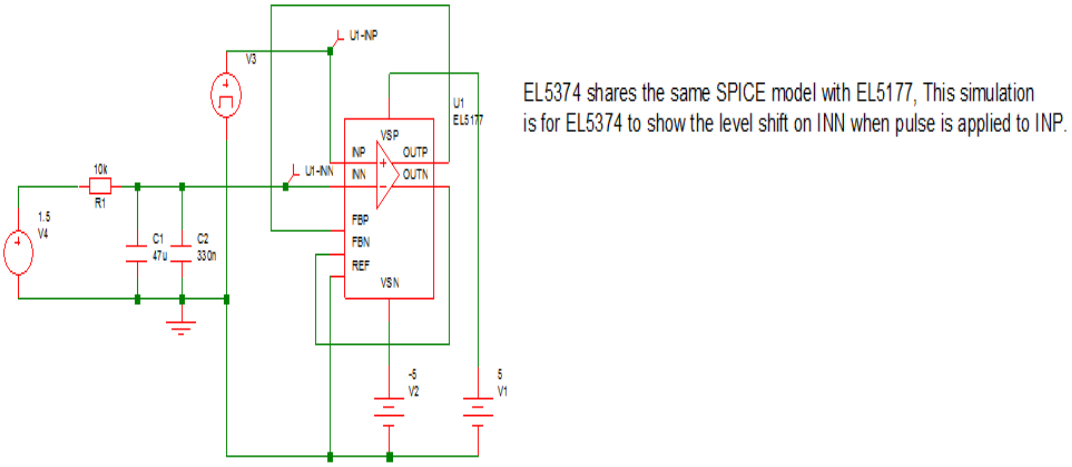


Figure 3.49 Peak shifting. (a) Spectra of Co at 0.5 µs shaping time as incident photon intensity changes from 1k to 20k, 40k, 80k, peaks of Co emission lines shift. (b) Expansion of Figure 3.49 (a) after normalization clearly shows the peak shifts.

(a)



(b)

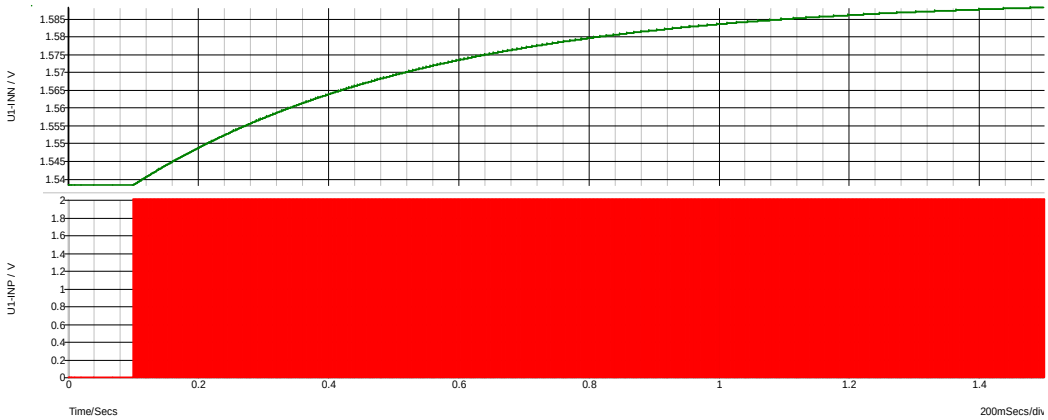
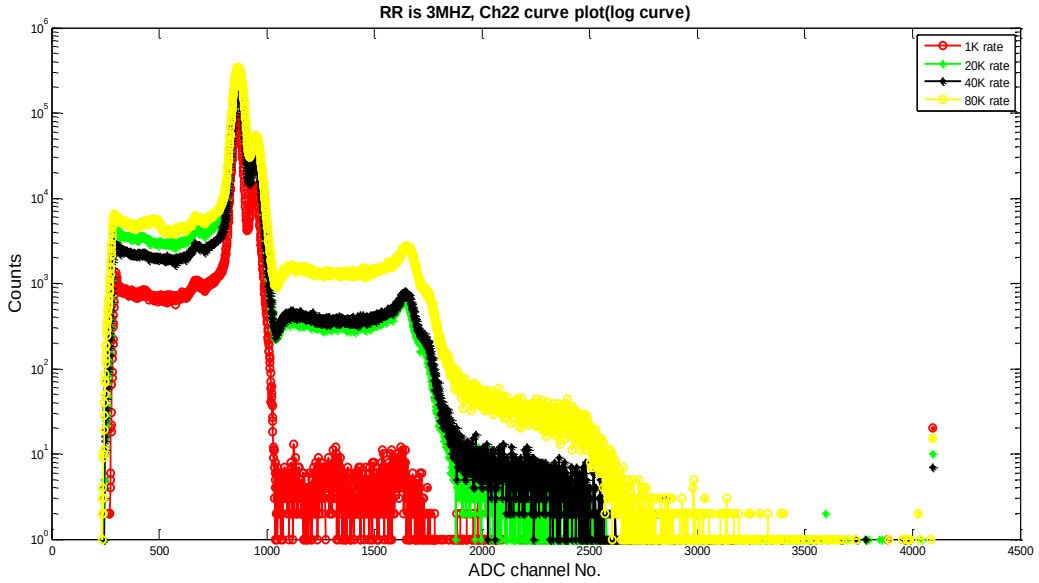


Figure 3.50 Psipice simulation for peak shifting. (a) Psipice simulation circuit for 1.5V bias at differential driver (EL5374), 1.5V is connected with INN pin of EL5374 (U1), 100k Hz square wave is connected with INP. The probes are connected with INP and INN of U1. (b) Pspice simulation result shows that there is 45mV shift on INN of U1 if 100k Hz square wave is applied to the differential driver.

(a)



(b)

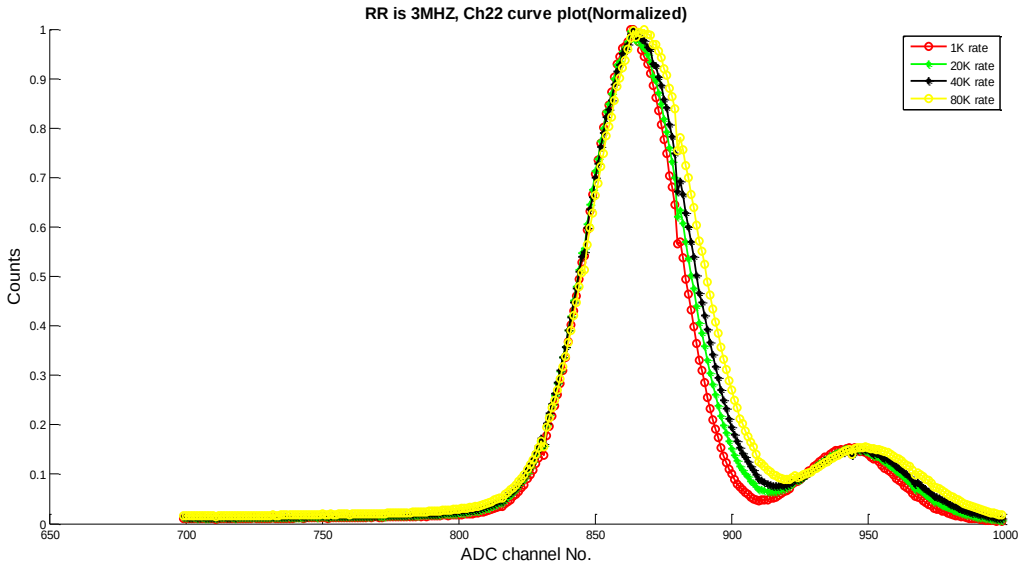


Figure 3.51 Peak shifting problem solved**.** (a) Spectra of Co at 0.5 µs shaping time as incident photon intensity changes from 1k to 20k, 40k, 80k. Peak shift of Co emission lines are almost negligible. (b) Expansion of Figure 3.51 (a) after normalization.

3.3.4 Application

A filter with dust from Tiernan Hall was tested with the 96 element detector to evaluate performance at low counting rates for low level atomic detection. The beam energy was

21 keV. The counting rate of incident photon to the detector is about 1k counts/s. Channel 22 is selected for analysis. The shaping time is 2 μs.

(a) (b) (c)

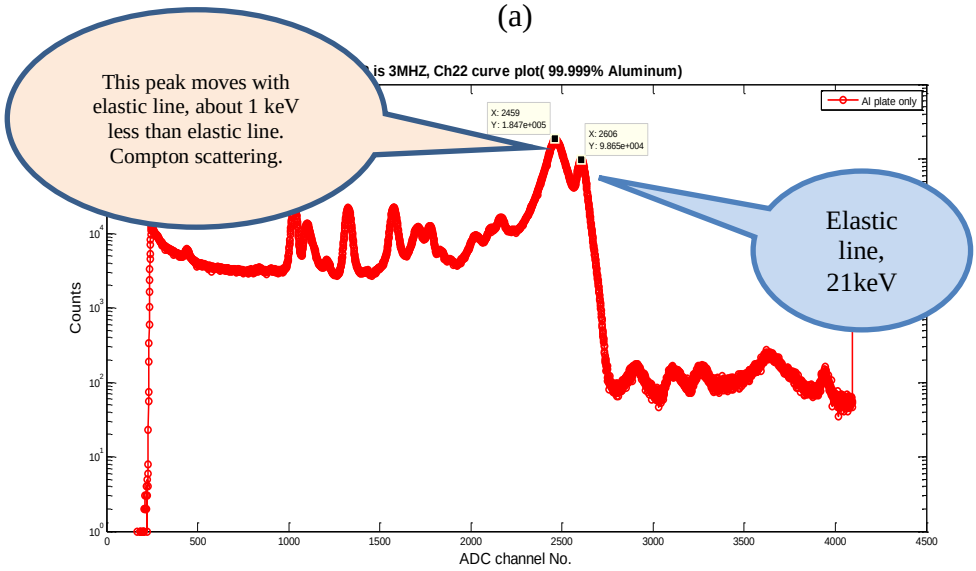
Figure 3.52 Filter samples and holder. (a) Clean filter sample. (b) Filter sample with dust from NJIT Tienan Hall. (c) 99.999% aluminum plate where sample will be placed

The 99.999% clean aluminum plate ($1/10^5$ impurity level) displayed in Figure 3.52 (c) is used as the background where the sample of clear filter (Figure 3.52 (a)) or dirty filter (Figure 3.52 (b)) is placed. Figure 3.53 (a) is the spectrum of the aluminum plate, most of the emission lines are from background including Pb tape. Figure 3.53 (b) is the spectrums of the clean filter and dirty filter. Figure 3.54 (a) is the spectrums which are normalized at the elastic peak (21 keV). Figure 3.54 (b) is the plot of data = filter with dust - clean filter data - minimum (filter with dust - clean filter) on a linear scale. The emission lines from the dirty filters are seen above the reference lines of the clean filter in Figure 3.54 (a); their existence is further proved in Figure 3.54 (b). Based on the E calibration, the elements in the dust are Fe and Zn.

Table 3.9 The Peak positions of Emission Lines of Dirty Filter Different from the Clean Filter

Peak position (ADC channel)	Energy (eV)	Element name
838	6389	Fe K_α
914	7027	Fe K_β
1100	8590	Zn K_α
1214	9547	Zn K_β

(a)



(b)

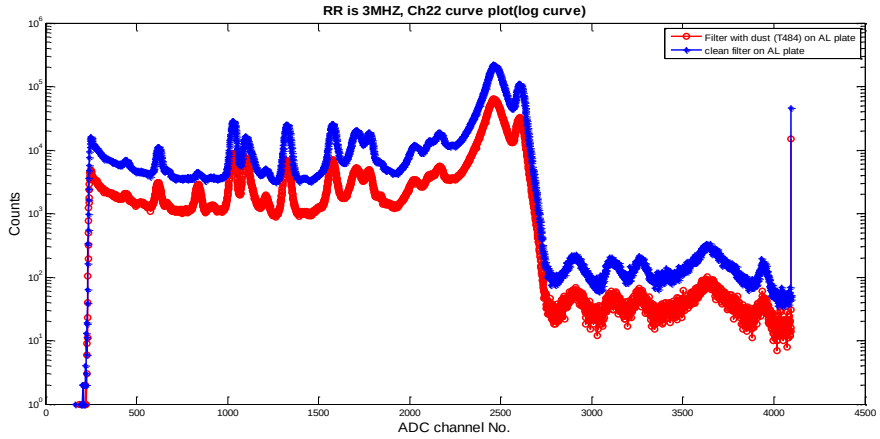
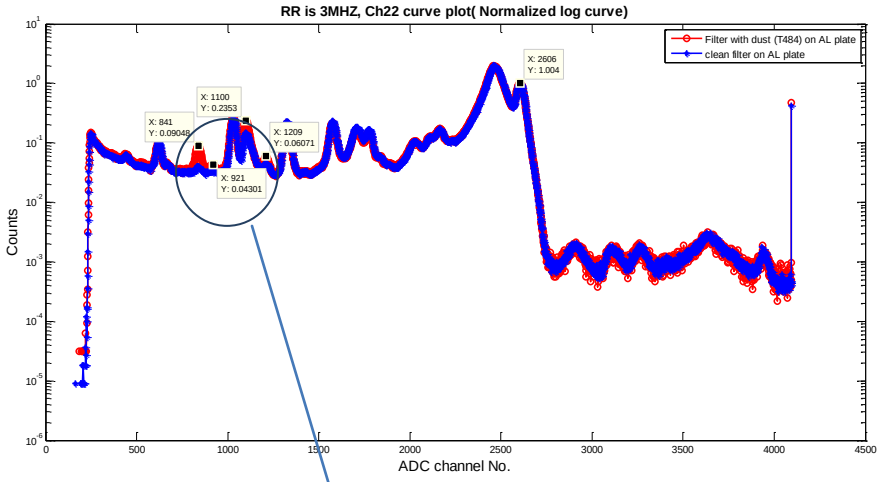


Figure 3.53 (a) The spectrum from detector when only the 99.999% aluminum plate is tested as the sample. The emission lines are from the background. (b) Spectrum of clear filter and filter with dust. In both figures, the incident energy is 21 keV.

(a)



(b)

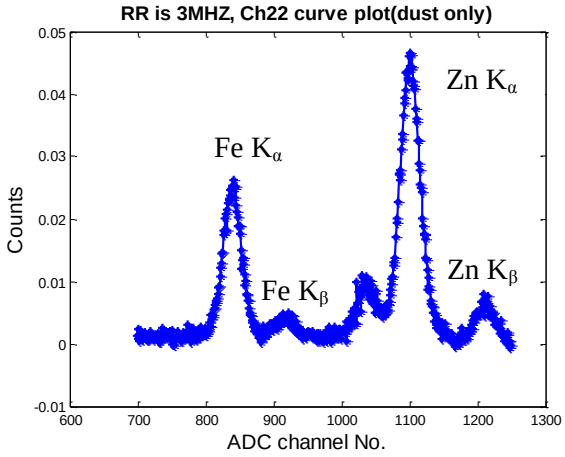
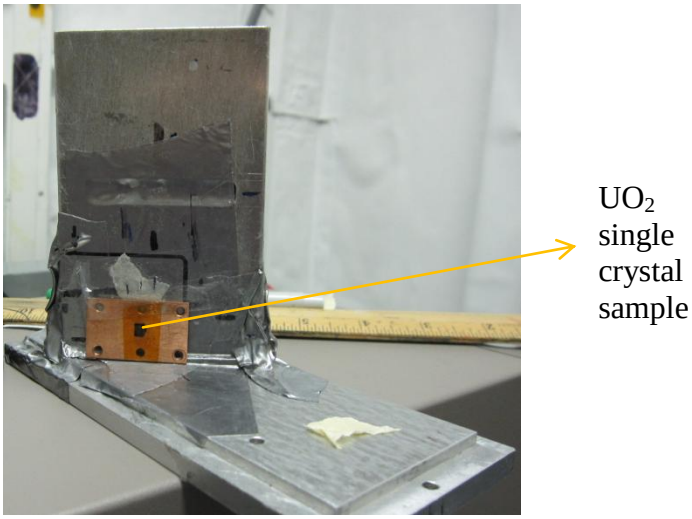
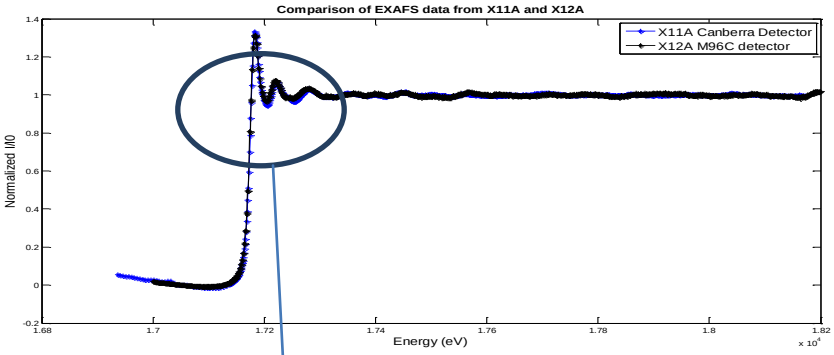


Figure 3.54 Spectrum analysis of filter with dust**.** (a) Spectrums of clean filter and filter with dust which is normalized at the elastic incident energy peak. (b) Plot (on linear y-scale) of data with dust after subtracting the spectrum of the clean filter. Note the prominent K emission lines from Fe and Zn.

(a)



(b)



(c)

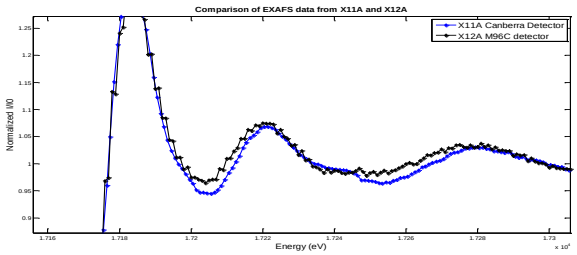


Figure 3.55 (a) UO_2 single crystal sample. (b) EXAFS of sample at U L3 edge (background subtracted and normalized) where the black curve is from the Maia 96 element detector with one scan and the blue curve is for the same sample measured at X11A with Canberra Ge detector with 4 scans. (c) The blue curve has bump in it.

The detector was also used for an EXAFS experiment. The sample was a UO_2 single crystal and the absorption as function of energy (U L3 edge) is plotted in Figure 3.55 (a). The black curve is from the Maia 96 element detector and blue curve is for the same sample measured at X11A with a 13-element Canberra Ge detector. The beam size was similar for both measurements yielding similar incident flux on the sample. The Maia data is for only one scan with 5 seconds per energy point while the X11A data is the average of 4 scans (taken at 3 sec per point up to 500 eV above the edge and 4 second from 500 eV to 1200 eV above the edge). Figure 3.55 (b) shows that the blue curve has bump in it (possibly a Bragg peak). Basing on this observation, it is concluded that data from the new Maia 96 element detector is much better.

3.3.5 Conclusions

The 96 element detector board was successfully developed. The detector analog board meets the expectations; the test results with either a laboratory (radioactive) radiation source or the synchrotron sources show that the best energy resolution approaches 230 eV at low counting rate; the intensity linearity is maintained at 0.5 μs shaping time when the output total counting rates go up to 40k counts/s (>5% bending point) when all pixels are active; the energy response is almost linear except at high energy end. The current detector, operating with a shaping time of 0.5 μs, can operate up to ~11 MHz total counting rate. It was found that when only 1 pixel is enable then the linear range can approach 200k counts/s. Hence the detector could reach 20M Hz theoretically. The bottleneck is the path delay between the SCEPTER chip of detector board and the high speed ADC of the DDM board.

In the fluorescence experiment with samples, the detectable energy ranges from Al K_{α} line to Uranium $L_{\Upsilon 1}$ line. The energy response can be slight modified to linear if linearization function of Maia system is applied. All the pixels show the similar response and after gain trim the data of all the pixels can be summed up to gain one spectrum without losing much resolution. Application tests of the detector were conducted to identify the elements in the dust; its spectrum shows that it contains the Fe and Zn. The EXAFS experiments were also conducted; the data of the detector is better than that of the Canberra detector at the X11A beamline.